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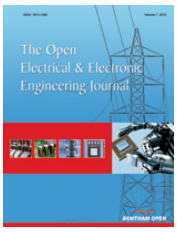

RESEARCH ARTICLE

Modeling and Controlling Strategy of Four-Switch Buck-boost Convertor with Smooth Mode Transitions

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Abstract: Four-switch synchronous buck-boost (FSBB) converter is much suitable for battery management system for its characteristic of wide input voltage range, high efficiency, and positive voltage output. A three mode control scheme with two modulation signals and one carrier can be adopted to achieve the smooth transition among modes. Using feed forward voltage mode control, the input voltage information is injected into the control loop to prevent the disturbance effect on the output voltage through making input voltage construct the carrier signal. High efficiency is gained when the converter is operating in pulse skip mode in light load. The operating mode smooth transition and stability could be achieved by modeling the converter and designing the compensation. Finally, a power prototype was fabricated to validate the validity of the control strategy.

Keywords: Four-switch synchronous buck-boost converter, Wide input voltage range, Three-mode smooth transition, Feed forward voltage mode control, Buck-boost (FSBB), SEPIC.

1. INTRODUCTION

With the wide use of portable electronics in modern society, the requirement of the power management system for the electronic equipment is demanding highly. Due to wide range of external charging power supply output voltage as well as the requirement of the conversion and use of power supply energy between various devices [1 - 3], buck converter or boost converter is needed to serve as a switching circuit for battery charging system [4, 5]. Given the wide input and output voltage range, single inductor four-switch Buck-Boost (FSBB) converter features simpler circuit, less devices and higher efficiency comparing with traditional buck-boost, Cuk, Zeta, SEPIC and other converters, which makes it not only suitable for portable electronics but also widely used in telecom power system, battery powered system and PFC power supply [6 - 8].

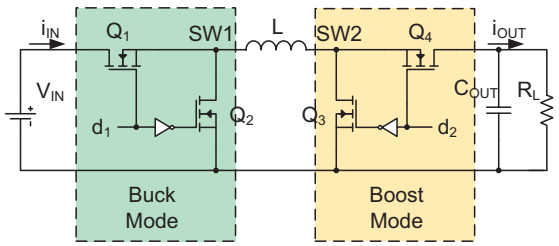

Fig. (1). FSBB converter.

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Fig. (**1**) shows the schematic diagram of single inductor four switch buck-boost converter, Q_1 and Q_3 are main power tubes, Q_2 and Q_4 are synchronous rectifiers. Comparing with traditional control mode that Q_1 and Q_3 must turn on and off at the same time, the control mode that Q_1 and Q_3 turn on and off respectively can effectively reduce the conduction and switching loss of the converter, and improve the efficiency [9 - 11].

When the input voltage is higher than the output voltage, the converter operates in buck mode [12 - 14]; When the input voltage is lower than the output voltage, the converter operates in boost mode [15 - 17]; Buck-boost operating mode is joined between two operating modes to achieve smooth transitions [18, 19].

2. TRANSITION PRINCIPLE OF OPERATING MODES

Fig. (**2**) shows the operation schematic diagram of double modulation-single carrier three mode transitions. V_{c_Buck} and V_{c_Boost} are control signals for buck and boost respectively, V_{bias} is the bias between the two control signals and V_M is the amplitude of carrier wave. Where $V_{c\_Buck} = V_{c\_Boost} + V_{bias}$, $V_{bias} < V_M$

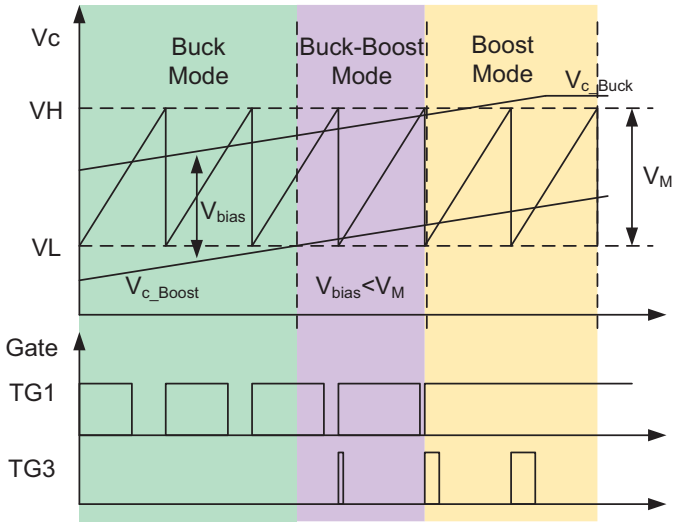


Fig. (2). Switching schematic diagram of operating mode.

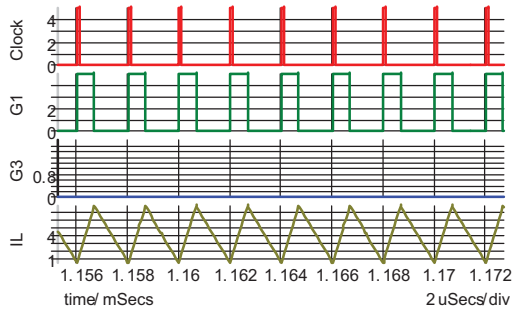
When $V_L < V_{c\_Buck} < V_H$, $V_{c\_Boost} < V_L$, the converter is on buck mode, duty ratio d_1, which is needed in this mode, is generated through contrasting V_{c_Buck} and carrier signal, thus Q_3 open and Q_4 close. When $V_L < V_{c\_Buck} < V_H$, $V_L < V_{c\_Boost} < V_H$, the converter is on buck-boost mode, duty ratio d_1 and d_2, which are needed in this mode, is generated through contrasting V_{c_Boost}, V_{c_Buck} and carrier wave; When $V_H < V_{c\_Buck}$, $V_L < V_{c\_Boost} < V_H$, the converter is on boost mode, while Q_1 close and Q_2 open, duty ratio d_2 is generated through contrasting V_{c_Boost} and carrier wave [12, 13].

Fig. (**3**) shows the simulation wave of those three operating modes, G_1 and G_3 are driver signals for Q_1 and Q_3 respectively, I_L is inductance current waveform.

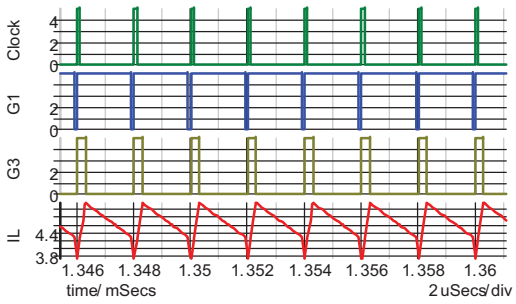
The simulation wave of converter is shown as Fig. (**3a**) when input voltage Vin=20V,output voltage Vout=12V, load I_{out}=4A, and converter is on buck mode.

The simulation waves of converter are shown as Fig. (**3b**) when Vin=11V, Vout=12V, Iout=4A and converter is on buck-boost mode. The simulation waves of converter are shown as Fig. (**3c**) when Vin=8V, Vout=12V, Iout=4A and converter is on boost mode.

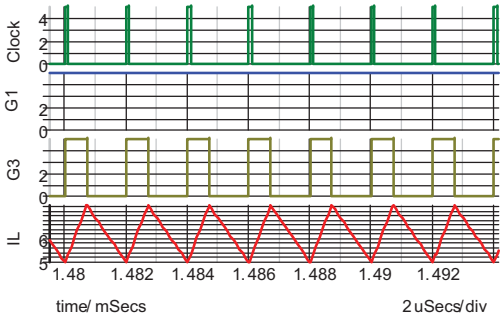
Though the simulation waves, we can see that comparing with traditional control mode, this working mode has lower switching loss when converter works on Buck or Boost mode, and lower conduction loss for the lower current effective value when the converter works on Buck-Boost mode.



(a) Buck operating mode



(b) Buck-Boost operating mode



(c) Boost operating mode

Fig. (3). Three working modes.

3. CONTROLLING STRATEGY AND MODELING FOR SINGLE-INDUCTOR FSBB CONVERTER

Fig. (**4**) shows the schematic diagram of voltage mode control FSBB converter. It can be seen from the figure that the output of the error amplifier generates two modulating signals, V_{c_buck} and V_{c_boost} through the bias voltage, and the needed driver signal is generated by the contrast between these two modulating signals and the same carrier signal. In order to restrain input voltage influence on output voltage [14 - 16], we introduce feed forward control and make input voltage constitute carrier signal through a integral circuit. When input voltage change, control signal can also rapidly change to restrain the influence of input voltage disturbance.

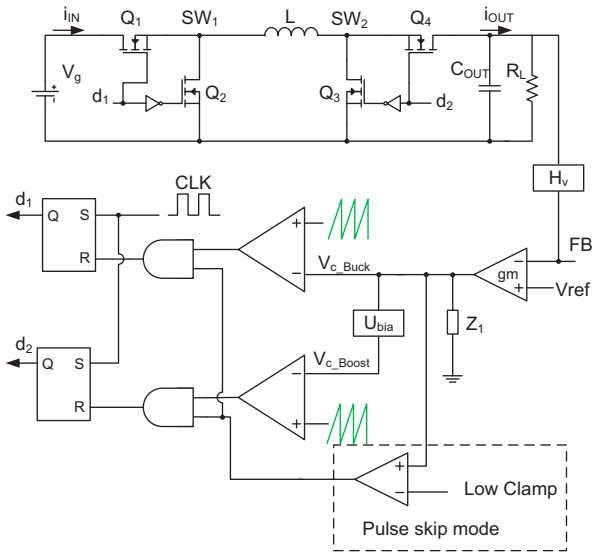


Fig. (4). FSBB converter based on voltage mode control.

Equation (1) shows the formula of carrier signal:

$$v_{ramp} = \frac{1}{RC} \cdot \int_0^t v_{in}(\tau) d\tau, 0 \le \tau \le T_s \quad \textbf{(1)}$$

When input voltage held constant, carrier signal V_{ramp} is a set of periodic saw tooth signal, duty ratio control signal d_1 and d_2 are generated by modulating signal, V_{c_Buck} and V_{c_Boost} and carrier signal V_{ramp}. Equation (2) shows the formula of PWM modulator:

$$d(t) = \frac{v_c(t)}{s_n \cdot T_s} \quad \textbf{(2)}$$

Where $v_c(t)$ denotes modulating signal, and $s_n = \frac{v_{in}(t)}{RC}$ is carrier slope. It can be seen from formula (2), output signal d of PWM modulator is the function of v_{in} and v_c, $d = f(v_c, v_{in})$, so the gain expression of PWM modulator in complex frequency domain is:

$$\hat{d}(s) = \frac{\partial d}{\partial v_c}\hat{v}_c(s) + \frac{\partial d}{\partial v_{in}}\hat{v}_{in}(s) = \frac{RC}{T_s \cdot V_{in}} \cdot \hat{v}_c(s) - \frac{RC \cdot V_c}{T_s \cdot V_{in}^2} \cdot \hat{v}_{in}(s) \quad \textbf{(3)}$$

In the steady-state,

$$V_c = \frac{V_{in}}{RC} \cdot DT_s + V_L \quad \textbf{(4)}$$

V_L is the low clamping voltage of V_c

Substituting (4) into (3):

$$\hat{d}(s) = \frac{RC}{T_s \cdot V_{in}} \cdot \hat{v}(s) - \left(\frac{D}{V_{in}} + \frac{V_L RC}{T_s V_{in}^2} \right) \hat{v}_{in} \quad \textbf{(5)}$$

Fig. (**5**) presents the control block diagram of converter voltage closed-loop [8]. $G_{vd}(s)$, $G_{vg}(s)$ and $Z_{out}(s)$ are the transfer functions from duty ratio $\hat{d}$, input voltage $\hat{v}_g$ to output voltage $\hat{v}_o$ and output impedance respectively, H(s) is the sampling function of output voltage, $G_v(s)$ is the compensation function of voltage loop, F_m is the gain of PMW modulator and k is the input voltage feed forward gain.

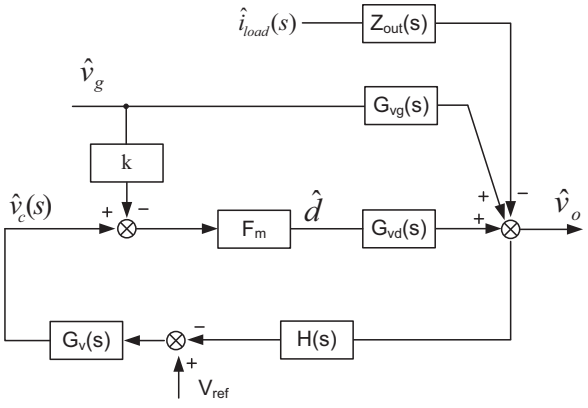


Fig. (5). FSBB converter control configuration.

The value of the gain of PMW modulator, F_m and feedforward input voltage, k can be derived by equation (5).

$$F_m = \frac{RC}{T_s V_{in}} \tag{6}$$

$$k = \frac{DT_s}{RC} + \frac{V_L}{V_{in}} \tag{7}$$

When the converter works on buck mode, transfer function from duty ratio to output voltage is:

$$G_{vd\_buck}(s) = \frac{V_{out}}{D} \cdot \frac{1}{1 + \frac{s}{Q_1 \omega_{o\_buck}} + \frac{s^2}{\omega_{o\_buck}^2}} \tag{8}$$

The transfer function from input voltage to output voltage is:

$$G_{vg\_buck}(s) = \frac{D}{1 + \frac{s}{Q_1 \omega_{o\_buck}} + \frac{s^2}{\omega_{o\_buck}^2}} \tag{9}$$

Where $Q_1 = R_L \sqrt{\frac{C_{out}}{L}}$, $\omega_{o\_buck} = \frac{1}{\sqrt{LC_{out}}}$

When the converter works on boost mode, transfer function from duty ratio to output voltage is:

$$G_{vd\_boost}(s) = \frac{V_{out}}{1-D} \cdot \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q_2 \omega_{o\_boost}} + \frac{s^2}{\omega_{o\_boost}^2}} \tag{10}$$

The transfer function from input voltage to output voltage is:

$$G_{vg\_boost}(s) = \frac{1}{1-D} \cdot \frac{1}{1 + \frac{s}{Q_2 \omega_{o\_boost}} + \frac{s^2}{\omega_{o\_boost}^2}} \tag{11}$$

Where $Q_2 = (1-D) R_L \sqrt{\frac{C_{out}}{L}}$, $\omega_z = \frac{(1-D)^2 R_L}{L}$, $\omega_{o\_boost} = \frac{(1-D)}{\sqrt{LC_{out}}}$.

The buck-boost working mode is the transition stage between buck and boost mode, and it has similarity on control loop with boost mode, so we take buck-boost working mode into boost mode to analyze.

Whether converter works on Buck mode or Boost mode, the system is a second-order system; in order to guarantee the stability of the converter, we use III type compensator to compensate converter. Fig. (**6**) gives the type-III compensator.

Complex frequency domain expression of the type-III compensator is:

$$G_c(s) = -\frac{(R_z C_z s + 1)[(R_1 + R_3) C_{ff} s + 1]}{R_1 \cdot s[R_z C_z C_p s + (C_p + C_z)](R_3 C_f s + 1)} \tag{12}$$

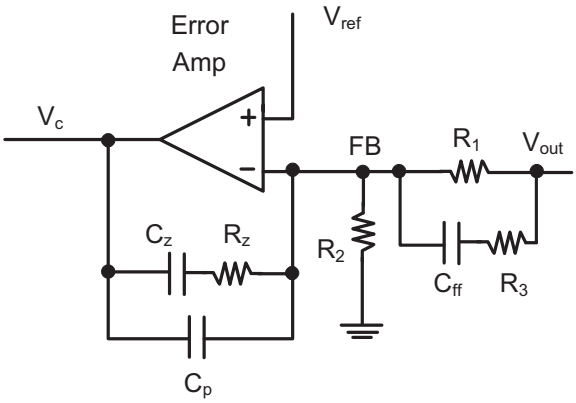
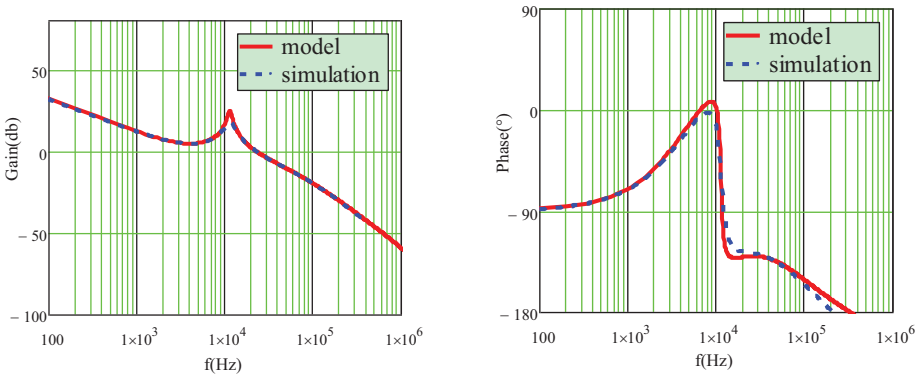


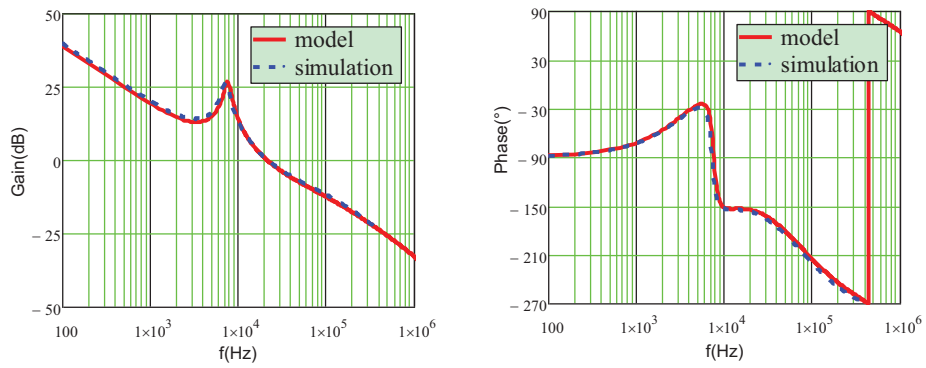
Fig. (6). Type-III compensator.

Pole at the base point of the compensator raises DC gain of the system, and reduces the steady state error of converter output voltage. Setting the two zero points at prior to the LC resonant frequency reduces influence of the system LC pole pair, and improves the phase margin. Setting the two poles at the rear of the half switching frequency, the two high-frequency poles rapidly downgrade high frequency gain and restrain high frequency noise.

To stabilize the buck and boost mode, we need to minish the Q value of buck and boost mode in addition to the compensation. Equations (8) and (10) above have made it clear that one needs to decrease the output capacitance or increase inductance to minish Q value. In the boost mode, however, an increased inductance would lead to shift of the right half plane zero point toward low frequency, thus causing decrease of phase margin and instability of boost mode. Therefore, the value of inductance should be modest.



(a) Buck mode



(b) Boost mode

Fig. (7). Modeling and simulation Bode diagram under different modes.

As shown in Fig. (**7a**), the Bode diagram of loop modeling and simulation in buck mode, the small-signal model of buck mode is consistent with the simulation, indicating that the small-signal model is precise. Here the cross-over frequency $f_c = 22kHz$, and the phase margin $P_m = 53°$.

As shown in Fig. (**7b**), the Bode diagram of loop modeling and simulation in boost mode, the right half plane zero point restrained the phase margin raising effect brought by the feedforward capacitance compensation, leading to decrease of phase margin in boost mode. Here the cross-over frequency $f_c = 22kHz$, and the phase margin $P_m = 28°$.

Fig. (**7**) indicates that cross-over frequency of the system is low in both buck mode and boost mode, thus the input voltage dynamic response is weak, and we need to introduce the input voltage to feedback loop to increase the dynamic response performance. Fig. (**5**) presents the block diagram of control of buck-boost converter, indicating that the open-loop gain of the voltage loop is:

$$T_v(s) = H(s)G_v(s)F_m G_{vd}(s) \tag{13}$$

When there is no input voltage feedforward, the closed loop transfer function from input voltage to output voltage is:

$$T_{vv}(s) = \frac{G_{vg}(s)}{1 + T_v(s)} \tag{14}$$

When there is input voltage feedforward, the closed loop transfer function from input voltage to output voltage is:

$$T_{vvff}(s) = \frac{G_{vg}(s) - kF_m G_{vd}(s)}{1 + T_v(s)} \tag{15}$$

Equations (15) and (14) lead to:

$$\frac{T_{vvff}(s)}{T_{vv}(s)} = \frac{G_{vg}(s) - kF_m G_{vd}(s)}{G_{vg}(s)} \tag{16}$$

When the buck-boost converter is operating in buck mode:

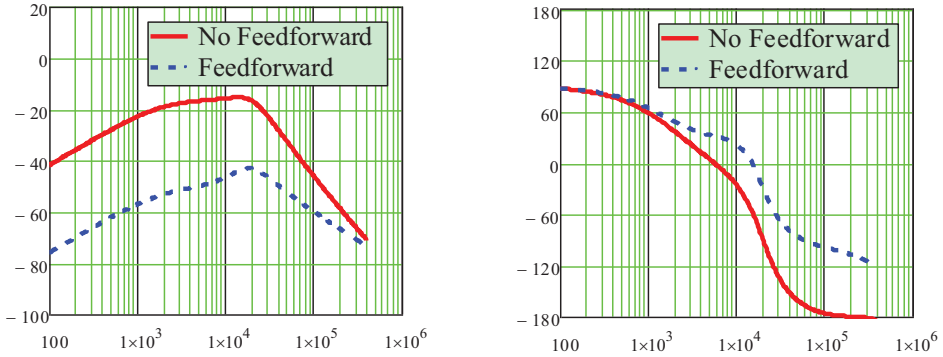
$$\frac{T_{vvff}(s)}{T_{vv}(s)} = -\frac{V_L RC}{T_s V_{out}} \tag{17}$$

When the buck-boost converter is operating in boost mode:

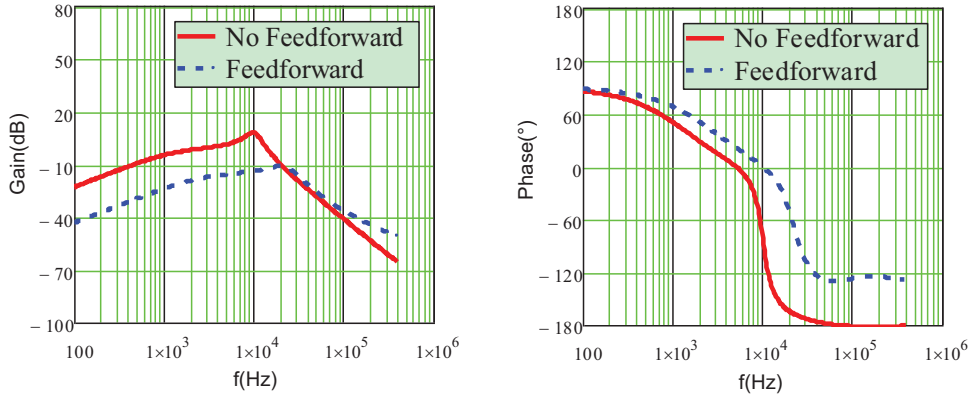
$$\frac{T_{vvff}(s)}{T_{vv}(s)} = 1 - \left(\frac{DV_{out}}{V_{in}} + \frac{RC}{T_s} \cdot \frac{V_L V_{out}}{V_{in}^2} \right) \cdot \left(1 - \frac{s}{\omega_z} \right) \tag{18}$$

Low clamp value of control signal Vc is generally small during the design process. Equations (17) and (18) indicate that when the input voltage is introduced in the feedback loop, closed loop gain from input to output of buck-boost converter decreases. It is showing that the input voltage feedforward control restrained the influence of input voltage disturbance on the output voltage.

Fig. (**8**) demonstrates the Bode diagram of closed loop transfer function from input voltage to output voltage in buck mode and boost mode. As shown in the figure, gain obviously decreases after the input voltage is added in the feedback loop, indicating that the system can effectively restrain the affect of input voltage disturbance on output voltage.



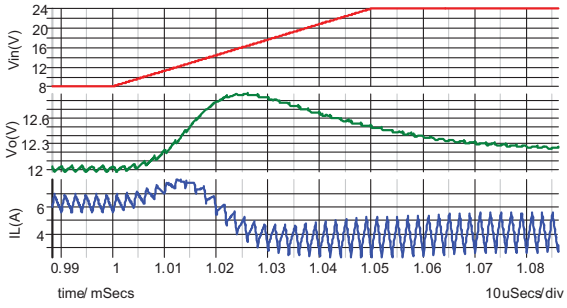
(a) Buck mode



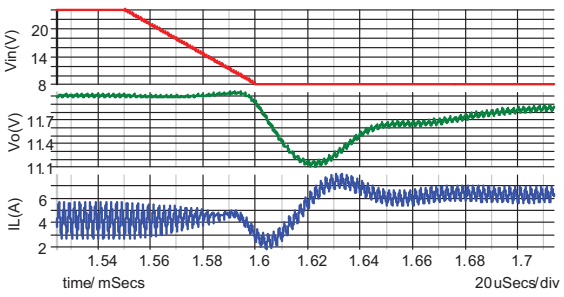
(b) Boost mode

Fig. (8). Bode diagram of closed loop transfer function from input voltage to output voltage under different modes.

Fig. (**9**) illustrates the system line transient response when its input voltage is jumping between 8V-24V. The figure indicates that the system operation is shifting smoothly among the three operation modes during line transient. When input voltage jumps from 8V to 24V, converter operates in buck mode, buck-boost mode and eventually works in boost mode. When input voltage jumps from 24V to 8V, converter operates in boost mode, buck-boost mode and eventually works in buck mode. During line transient, the change of output voltage is within ±8%, which meets the system operation requirement.



Waveform of input voltage jumping from low to high



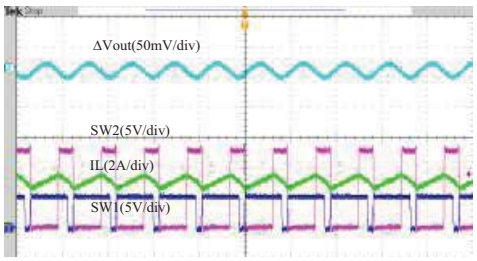
Waveform of input voltage jumping from high to low

Fig. (9). Line transient response.

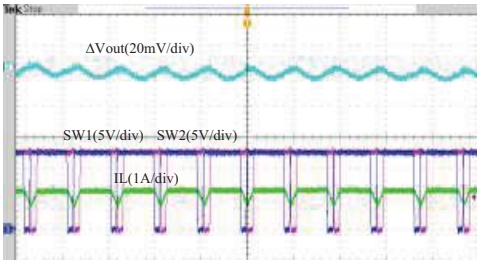
4. EXPERIMENT VALIDATION

An experimental prototype was set in laboratory condition to verify the performance of the prototype under the control strategy proposed in the paper and the compensation parameters. Major parameters of the prototype are as follows: Vin=3V-36V, Vout=12V, L=4.4uH, Cout=44uF, Rz=50kΩ, Cz=680pF, Cff=470pF, Cp=5pF°.

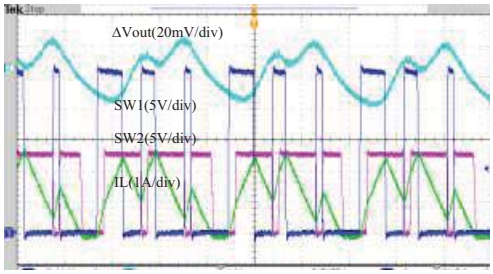
Fig. (**10a**) presents the steady state experiment waveforms under different operation modes. Fig. (**10b**) shows the experiment waveform under buck-boost mode, where the waveform of inductance current is a trapezoidal wave; compared to the triangular wave under the same load, the inductance current RMS value decreases, and so does the system conduction loss. Fig. (**10c**) presents the experiment waveform in boost mode. When the system works in light load, to reduce system loss, it works in pulse skip mode; therefore, during the critical conduction, slight vibration occurs due to the inter-affect between pulse skip loop and continuous conduction control loop.



(a) Experiment waveform in buck mode



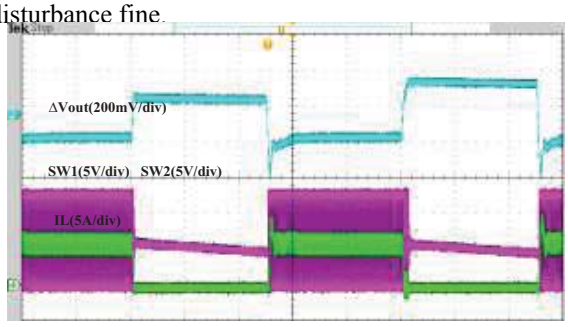
(b) Experiment waveform in buck-boost mode



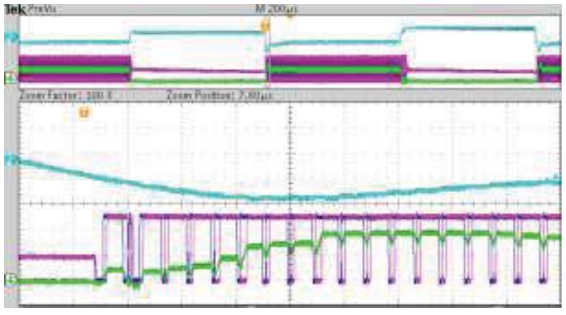
(c) Experiment waveform in boost mode

Fig. (10). Steady state experiment waveform.

Because the buck-boost mode is actually the transition between buck mode and boost mode, it is also an unstable zone of the system. Fig. (**11**) gives the test on load transient response in buck-boost mode. As shown in the figure, when the load jumps between 0 and 5A, the output voltage stays stable within ±5%, indicating that the system bandwidth is reasonable; in the meantime, no vibration occurs, showing that the system has enough phase margin and restrain input disturbance fine.



(a) Experiment waveform of load transient



(b) Zoom in waveform

Fig. (11). Experiment waveform of load transient.

CONCLUSION

In the study, different operation modes of four-switch Buck-Boost (FSBB) converter were modeled, and the accuracy of the models were verified through loop simulation. Voltage mode control has weak restrain effect over input voltage disturbance. To solve the problem, we constructed carrier signal with input voltage to introduce the input voltage into feedback loop, and restrained the disturbance of input voltage. Simulations showed that, with reasonable parameter design and input voltage feedforward, the phase margin of system has been increased, and the stability was raised. At last we designed an experimental prototype with input voltage between 3V-36V and output voltage 12V for test. Test results showed that the system can shift in the three modes smoothly, that the compensation parameters were rational, that the bandwidth was high, and that the phase margin was enough.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

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