Status of the Emerging InAlN/GaN Power HEMT Technology

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Abstract: The InAlN/GaN heterojunction appears to be a new alternative to the common AlGaN/GaN configuration with higher sheet charge density and higher thermal stability, promising very high power and temperature performance as well as robustness. This new system opens up the possibility to scale the barrier down to 5 nm while maintaining nearly its ideal materials and device properties. The status, focussing on the lattice matched materials configuration, is reviewed.

INTRODUCTION

Increasing demand for high power amplifiers in wireless communication systems and radars has stimulated new developments in solid state device structures. One emerging area had been gallium nitride (GaN) based FETs. Its large bandgap, high breakdown field, high electron mobility and its ability to form heterojunctions in the (In, Al, Ga)N materials matrix are its attractive properties in comparison to conventional gallium arsenide pseudomorphic-HEMTs. In the last decade, outstanding performance has been demonstrated with AlGaN/GaN HEMTs [1,2], yielding in the highest microwave power handling capability of all solid state device configurations up to now.

Besides the wide bandgap the main advantage of this AlGaN/GaN heterostructure had been the polarization induced 2DEG-channel charge density. Two polarization effects contribute. These are the difference in spontaneous polarization of GaN and AlGaN respectively and the piezo-polarization induced by the strain of the lattice mismatched heterostructure. At 30 % Al-content the two contributions are roughly equal.

In spite of the excellent device and circuit demonstrations, there have been only a limited number of published reports regarding the reliability of the AlGaN–GaN HEMT technology [3]. Recently, the lack of reliability of AlGaN/GaN devices has been explained by lattice defects introduced by the stress resulting from the mismatch and modulated by the piezoelectric effect [4]. However, the device performances and reliability may still be further improved by substituting the AlGaN barrier by InAlN. Indeed, as can be seen from the composition diagram of the III-nitride materials matrix (Fig. **1**), InAlN can be grown lattice matched to GaN [5]. Thus, at this composition stress and piezo-polarisation are not present, potentially improving the stability of the heterostructure.

Even without piezo-polarization, the 2DEG-channel sheet charge density induced by the difference in spontaneous polarization is larger than typically in the AlGaN/GaN heterostructure. This should result in a higher output current density and, if the breakdown conditions can be preserved, even higher power density. The high Al-content places the InAlN alloy closer to AlN than the AlGaN alloy used in AlGaN/GaN FETs. AlN possesses the highest spontaneous polarisation in the materials matrix and a Curie temperature well above 1000°C, indicating a high chemical/thermal stability. In comparison, GaN decomposes in atmosphere at 650°C [6], although grown mostly at around 1000°C. Thus, InAlN/GaN heterostructure FETs may display a higher chemical/thermal stability than their AlGaN/GaN counterparts potentially allowing operation at higher temperature and improving robustness. A high chemical stability may also result in an improved control of the surface instabilities, plaguing polarization dipole induced channels. At the same time it may also allow to implement thinner barriers. In this paper these characteristics will be discussed to assess, whether the above mentioned improvements can indeed be expected.

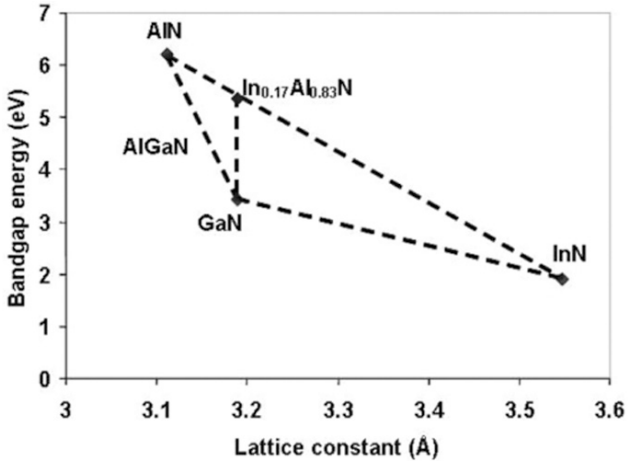

Fig. (1). GaN-based heterostructure materials matrix and polarization induced 2DEG charge densities.

MATERIAL PROPERTIES

The materials system is difficult to grow due to the distinctly different growth conditions required for GaN and

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InAlN and the difficulty to incorporate In and Al in the same lattice without clustering. Major issues concerning the growth of InAlN are the different requirements for the binaries contained in the ternary alloy, namely InN and AlN. AlN tends to grow polycrystalline for growth temperatures below 1000 °C [7]. On the other hand, InN can only be grown at low temperatures and high ammonia partial pressures, whereby high ammonia partial pressures have also a strong effect on the AlN growth rate. However, these problems have been widely overcome in first promising experiments [8-11]. In particular, it has been found that the insertion of an optimized AlN interlayer reduces the alloy related interface roughness and improves therefore the electron mobility dramatically as shown in Fig. (**2**). This enabled to obtain an electron mobility well beyond 1000 cm^2/vs in conjunction with a sheet carrier density up to 2.6×10^{13} cm^{-2}, resulting in typical sheet resistances of about 200 Ω/□.

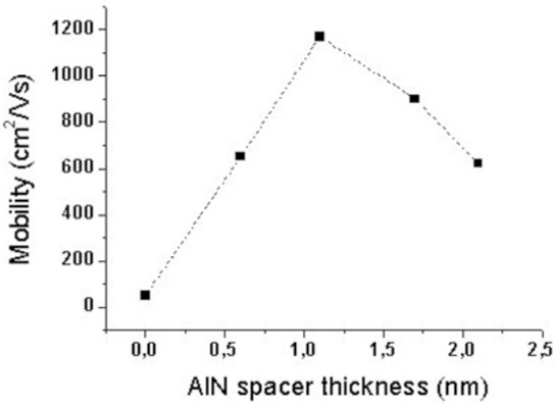

Fig. (2). Electron mobility as a function of the AlN spacer thickness.

The use of a high Al content in the barrier leads to an increase of the polarization discontinuity and thus to an even higher sheet carrier density and maximum output current density. An attractive approach with this new system is to decrease the In content in the barrier layer in order to come close to AlN, theoretically delivering the highest possible channel sheet charge density of more than 4×10^{13} cm^{-2}. Fig. (**3**) shows the experimental sheet carrier density (N_S) determined by Capacitance-Voltage measurements as a function

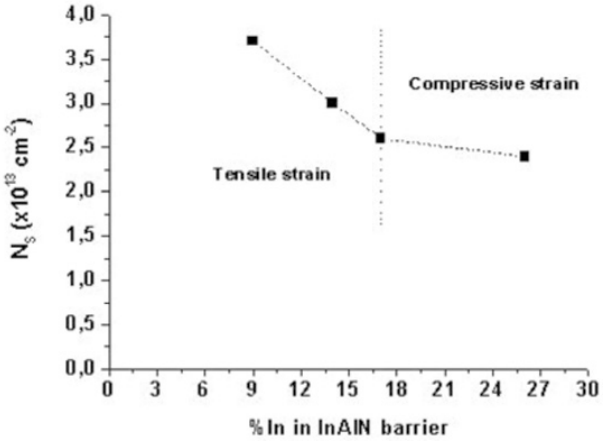

Fig. (3). Experimental N_S as a function of the In content in the InAlN barrier layer (C-V measurements).

of the In content of the InAlN barrier. Extremely high N_S close to 4×10^{13} cm^{-2} can be reached with less than 10 % In, which is approx. 3 times higher than typical AlGaN devices. With increasing Al-content the barrier becomes increasingly stressed, resulting in a critical thickness of only a few nm for AlN**.** Barrier layers with high Al-content must be therefore thin and AlN smoothing layers need to be considered. By respecting the critical thickness in order to avoid biaxial strain relaxation and cracking of AlN, extremely high sheet densities and room-temperature mobility exceeding 1000 cm^2/vs can be obtained with AlN/GaN configurations [12].

For AlGaN/GaN heterostructures the full interfacial 2DEG density (~10^{13} cm^{-2}) may become depleted for barrier thicknesses below approx. 25 nm due to a high surface potential often observed at approx. 1.5 eV below the conduction band edge, reducing the maximum accessible drain current density. This trap level may be removed by passivation [13,14] and thinner barriers become possible [15], but are not widely implemented. In the case of InAlN the surface potential of as-grown heterostructures is pinned at a level of approx. 0.4 eV and the barrier layer thickness can be scaled well below 25 nm [16], enabling planar high aspect ratio devices with nm gate lengths. In Fig. (**4**), the experimental N_S of lattice matched InAlN/GaN HEMTs are reported as a function of the InAlN barrier thickness. The 2DEG depletion occurs at a barrier thickness around 8 nm. It has to be stressed that still high N_S values of 1.7×10^{13} cm^{-2} are measured with a 5 nm InAlN barrier, demonstrating the possibility to grow extremely thin barrier while keeping high sheet carrier density.

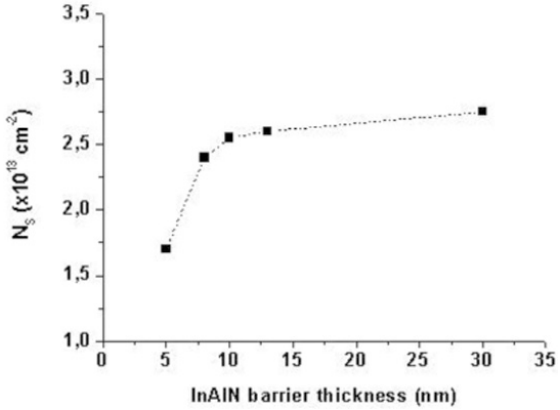

Fig. (4). Experimental N_S as a function of the InAlN barrier thickness (C-V measurements).

DEVICE TECHNOLOGY

The technology of InAlN/GaN FET devices follows many common processing steps of the AlGaN/GaN technology.

For ohmic contacts Ti/Al/Ni/Au is mostly used. However, InAlN is a very stable refractory compound and will not produce deep alloying profiles during contact annealing at around 850°C. The interfacial 2DEG channel needs therefore to be contacted directly by tunnelling and the metallization may need to be placed into a recess trench. Thus, many of the early FET output characteristics show slightly rectifying behaviour. However, the low surface potential of InAlN allows to design barrier layers, which approach the tunnel-

ling thickness, which then allows planar ohmic contact formation and low contact resistances down to 0.35 Ω.mm, but will also result in Schottky contacts with high leakage. In this case a dielectric assisted barrier is needed, leading to a MOSFET-like configuration. Fig. (**5**) shows the improvement in gate leakage when inserting a 5 nm Al_2O_3 gate dielectric into a MESFET with 13 nm InAlN barrier [17]. High-k dielectrics are of special interest like Al_2O_3 and HfO_2.

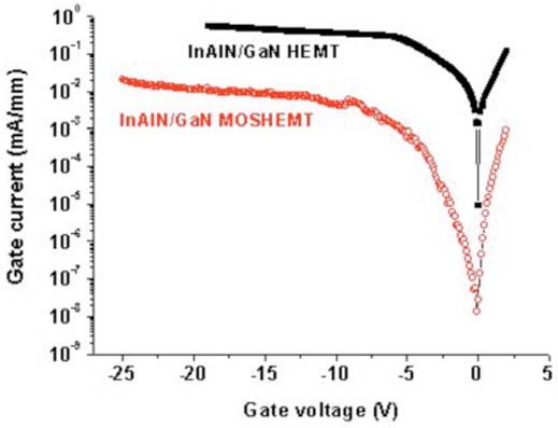

Fig. (5). Gate leakage of Ni/Au Schottky contacts of InAlN/GaN HEMTs with 13 nm barrier and with insertion of Al_2O_3 insulator as MOSHEMT.

DEVICE PERFORMANCES

DC Characteristics

One of the main advantages of the InAlN/GaN heterostructure is the high interfacial sheet charge density, which should enable extremely high current level density.

The first significant DC characteristics of unstrained InAlN/GaN HEMTs have been obtained on Si substrate [18], yielding a maximum DC output current at room temperature of I_{DS} = 1.8 A/mm at a gate bias V_G = +5 V with a peak transconductance g_m = 180 mS/mm. Recently, the electron mobility improvement associated with a high 2DEG density has enabled to achieve more than 2 A/mm (see Fig. **6**) using a lattice matched InAlN/GaN HEMT on sapphire with 13 nm barrier and 0.25 μm gate length. This value is about twice as much as obtained for AlGaN/GaN FETs [19].

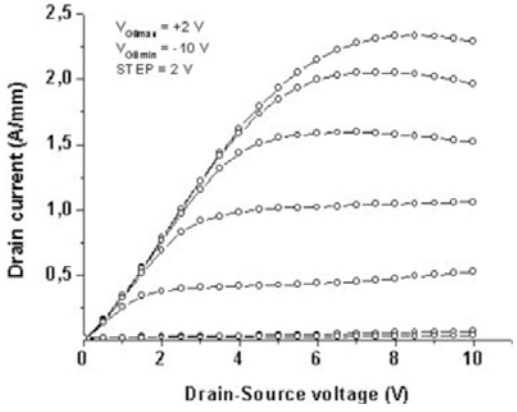

Fig. (6). Output characteristics of lattice matched InAlN/GaN HEMT with 13 nm barrier grown on sapphire. Gate length was 0.25 μm and gate width 25 μm.

The low surface potential allows down scaling of the barrier layer to the tunnelling limit and semi-enhancement mode of operation. Fig. (**7**) shows the output characteristics of devices with a gate length of 0.25 μm, fabricated on lattice matched heterostructures with 8 nm and 5 nm barrier layers respectively (adding a 1.0 nm AlN smoothing layer). As can be seen the maximum open channel current density (at V_G = +2 V) is slowly decreasing to 1.9 A/mm and 1.3 A/mm, in agreement with what can be expected from Fig. (**4**).

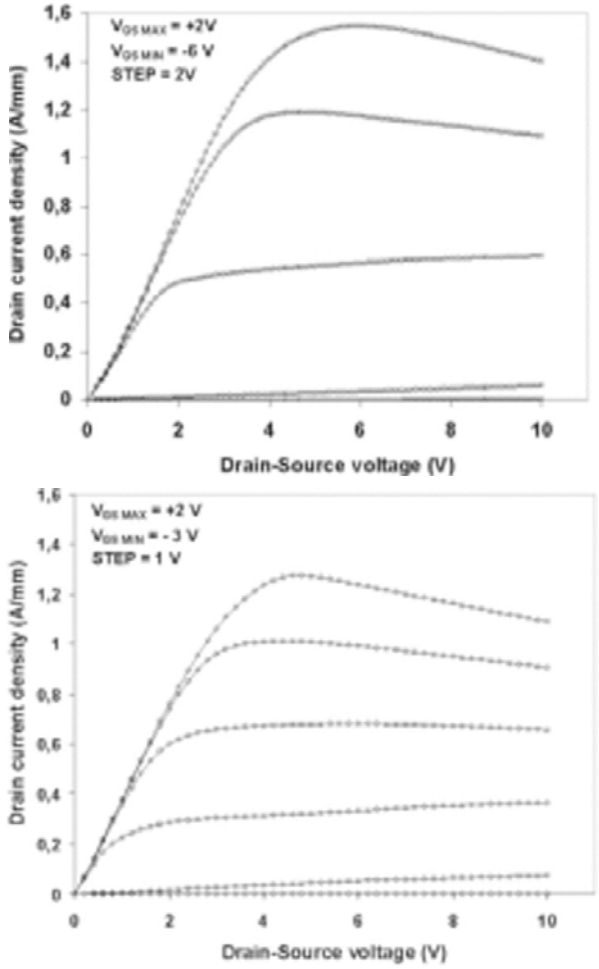

Fig. (7). Output characteristics of lattice matched HEMT structures of identical geometry and two different InAlN barrier thicknesses of 8 nm (top) and 5 nm (bottom). Also included is a 1 nm AlN smoothing layer.

The influence of the barrier thickness is also noticeable by the changes in threshold voltage and transconductance. Fig. (**8**) shows the dependence of the threshold voltage on the total barrier layer thickness. The scaling of the threshold voltage is indeed inversely proportional to the total barrier thickness. Enhancement mode of operation (V_{TH} = 0 V) can be predicted for a barrier thickness of approx. 2 nm, which would then be in combination with an extremely high channel sheet charge and maximum open channel current density. With thinner barrier also the peak transconductance is increased as shown by the transfer characteristics in Fig. (**9**). For the 5 nm barrier a peak transconductance of 505 mS/mm is obtained (L_g = 0.25 μm), which represents one of the highest of GaN-based FETs. Even higher transconductances

can be expected with thinner barrier. However to take advantage of such a structure, ultra short gate length (below 100 nm) must be used in order to respect the aspect ratio as mentioned in the next part. The depletion caused by the residual surface potential (which acts also as parasitic current limiter) would however still need to be overcome.

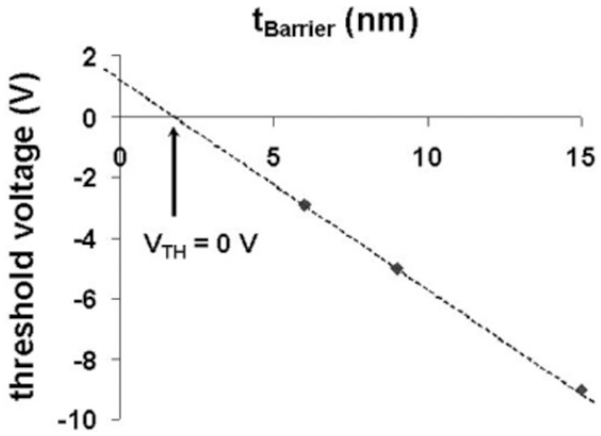

Fig. (8). Threshold voltage dependence on barrier layer thickness of lattice matched HEMTs.

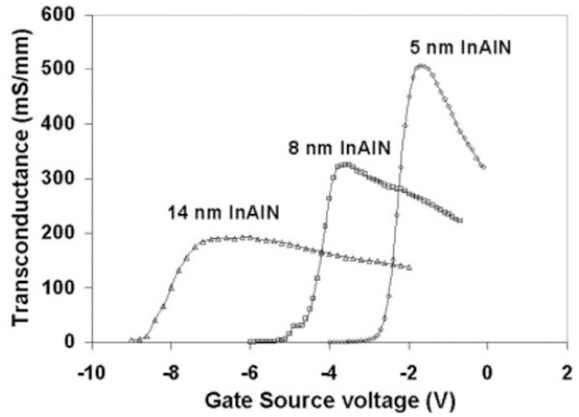

Fig. (9). Dependence of extrinsic transfer characteristics on barrier layer thickness of lattice matched InAlN/GaN HEMTs with 0.25 μm gate length.

DYNAMIC CHARACTERISTICS

In order to achieve high frequency performance, it is necessary to reduce the HEMT gate length while keeping an optimum aspect ratio (gate length on gate to channel distance), which has to be typically around 5 in the case of traditional GaAs and InP-based HEMT devices [20]. Lately, it has been demonstrated that the achievement of optimal frequency performance for GaN-based technology required a significantly higher aspect ratio of approx. 15 in order to mitigate the short channel effects at high drain bias [21]. For AlGaN/GaN devices, conventional barrier thicknesses are around 25 nm. This prevents the use of ultra gate length lower than 100 nm without the apparition of short channel effects [21]. A possibility to overcome this drawback is the use of a gate recess. However, the dry etching necessary for a gate recess of AlGaN is difficult to implement and degrades the surface underneath the gate, which may be detrimental for the Schottky diode quality and device reliability. Therefore, InAlN/GaN HEMTs will allow high aspect ratios with gate lengths lower than 100 nm, while maintaining a high sheet carrier density. The 2DEG mobility at the interface between the GaN buffer and the AlN smoothing layer is still slightly lower than in the case of AlGaN/GaN heterojunctions. The small signal microwave performance of InAlN/GaN HEMTs is for that reason very comparable with that of AlGaN/GaN HEMTs at similar gate length with an F_T = 53 GHz and F_{max} = 95 GHz for 0.2 μm gate length (and no T-gate). The same holds for the small signal performance for MOSHEMTs with a high-k gate dielectric like Al_2O_3 [19]. The current gain cut-off frequency F_T for different gate lengths of InAlN/GaN devices with 13 nm barrier thickness has been measured in order to emphasize the advantage of a high aspect ratio. Unlike typical AlGaN/GaN devices, an increase of F_T with the reduction of the gate length even with sub-100 nm gate length is observed and not masked by parasitics (see Fig. **10**).

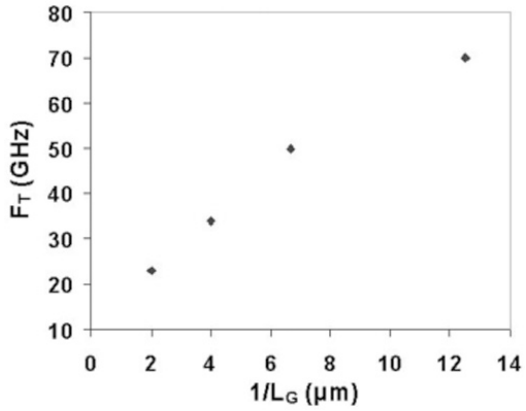

Fig. (10). Cut-off frequency performances of 13 nm barrier thickness $In_{0.19}Al_{0.81}N$/GaN HEMT biased at V_{DS} = 10 V for various gate lengths.

Likewise in AlGaN/GaN HEMT structures the large signal performance is largely affected by the polarization dipole characteristics and surface related instabilities like current compression or power slump, even when the buffer layer is stable. Many of the phenomena can be associated with surface charging effects between gate and drain commonly called “virtual gate” effect [22]. Here the origin of the instability is seen in the charging and discharging dynamics of the deep surface donor. In part, the charging path may be *via* generation/recombination in the barrier layer or *via* lateral surface leakage. This surface leakage may be strongly (gate to drain) field dependent and appears often as lateral charge injection from the gate metal contact into the adjacent surface of the drift region. Both effects are usually identified by pulsing the gate or drain bias respectively. Gate pulsing will therefore be mostly sensitive to traps in the barrier and buffer layer; drain bias pulsing will be especially sensitive to surface effects. At high drain bias high fields develop in the gate-drain drift region and there may be a threshold, when lateral surface charge injection and “drain-lagging” appears. For stable operation the InAlN surface needs to be characterized further and a clean interface to a wide bandgap high-k dielectric over-layer developed.

Pulse experiments reveal the same characteristics as seen in AlGaN/GaN HEMTs and depend essentially on the passivation technology used. First microwave power measure-

ments have still shown conservative results [23]. Nevertheless, more than 5 W/mm at 4 GHz has been recently obtained with a lattice matched structure using a SiN passivation without field plate technology at a drain bias V_{DS} = 30 V(see Fig. **11**). It has to be pointed out that this result has been performed with an open channel current level far below the potential of the structure (approx. 1.2 A/mm). Consequently, there is still room for improvement of InAlN/GaN HEMT power performance.

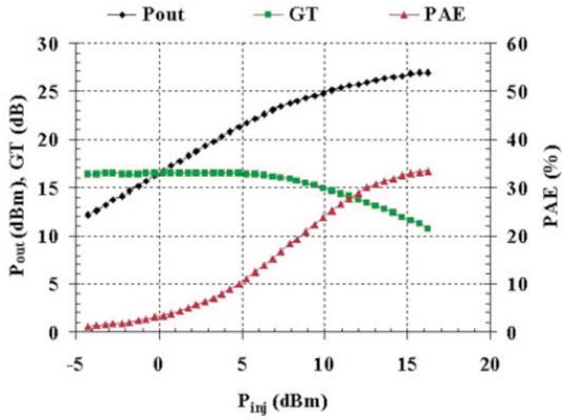

Fig. (11). Output power, gain, and power added efficiency at 4 GHz of a 0.25×100 μm^2 gate $In_{0.19}Al_{0.81}N$/GaN HEMT biased at V_{DS} = 30 V. The epi-layers used for these devices have been performed by Thales 3-5 lab (France) in Dr M.A. Poisson's group.

HIGH TEMPERATURE PERFORMANCE

The short time temperature stability of InAlN/GaN HEMT structures under DC operation has been tested in vacuum in a temperature ramping experiment [24].

Here the temperature was ramped in 100 °C steps with a time interval of 10 min at each temperature, where the DC output characteristics were taken with tungsten carbide test needles in the vacuum chamber. The temperature had been calibrated by several methods (thermocouple reading, pyrometer and melting point detection). At very high temperature, where the thermal losses are the highest, the temperature of the chip surface has been calibrated by melting of the Au contact metallization at 1063 °C. This was then compared to the thermocouple reading located within the substrate holder. Fig. (**12**) shows the device under test at 1000 °C.

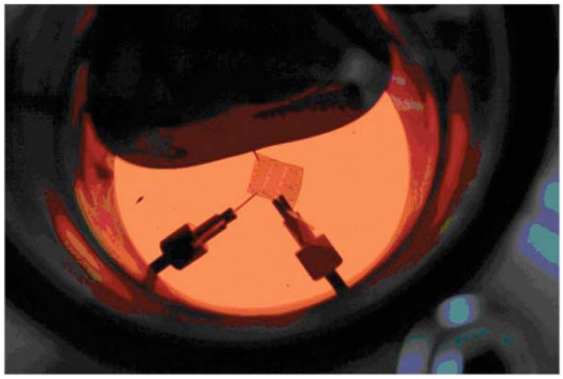

Fig. (12). HEMT device under test at 1000 °C in vacuum chamber.

Fig. (**13**) shows the output characteristic under open channel condition at V_G = +2 V and pinch off at V_G = -8 V for RT, 600 °C and 800 °C operation. It can be seen that ohmic and Schottky contacts are both highly stable. Schottky diode leakage does not prevent transistor operation even at 1000 °C (see Fig. **14**). In the linear region, the channel resistance is gradually increasing, indicating a reduction of mobility with temperature. Up to 600 °C residual barrier characteristics are still visible in the source and drain contact characteristics, which are overcome only at the highest operating temperature of 800 °C. At 600 °C the maximum output current is also only slightly reduced, indicating that operation up to this temperature may still be velocity saturation dominated. At 800 °C pinch-off is softened. Indeed operation at 1000 °C shows severe bypass conduction through the buffer layer. It seems therefore that the high speed performance at high temperature is influenced by two major factors. The reduction in mobility, so that velocity saturation will only dominate at reduced gate length; and secondly buffer layer leakage through trap activation resulting in a low output resistance. Especially the second effect will effectively limit the microwave performance of the device severely as was the case for the high temperature performance of GaAs FETs [25]. It is therefore a challenge to develop GaN buffer layer configurations, which remain semi-insulating at these high temperatures.

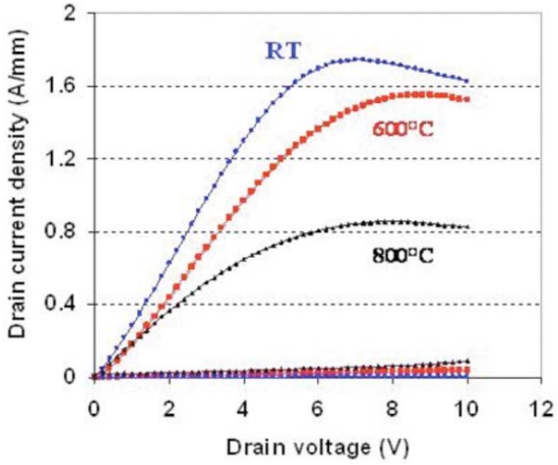

Fig. (13). Output characteristics of 0.25 μm gate length devices for V_G = +2 V (open channel) and V_G = -8 V (pinch-off) at room temperature, 600 °C and 800 °C.

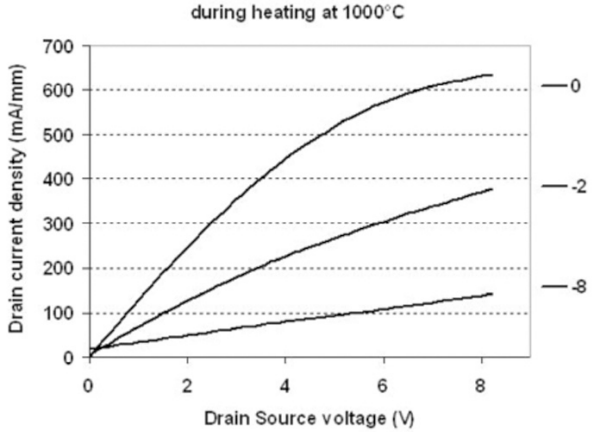

Fig. (14). Output characteristics of 0.25 μm gate length devices at V_G = 0 V, -2 V and -8 V (pinch-off) at 1000 °C.

Fig. (**15**) shows DC characteristics before and after the temperature cycling test up to 1000 °C. The original current level is restored. A slight decrease of the transconductance is observed due to a small degradation of the ohmic contacts. Thus, no major permanent degradation was observed. We attribute this high thermal stability to the chemical stability of the InAlN barrier layer and to the absence of strain in the InAlN/GaN heterostructure. HR-TEM (High Resolution Transmission Electron Microscopy) and EDX (Energy dispersive X-ray spectroscopy) of the interface between the Ni/Au Schottky contact and the InAlN/GaN heterostructure have been performed upon cooling from 1000°C (see Fig. **16**). No presence of Ni and Au has been detected in the InAlN layer which means that no noticeable inter-diffusion occurred at such a high temperature.

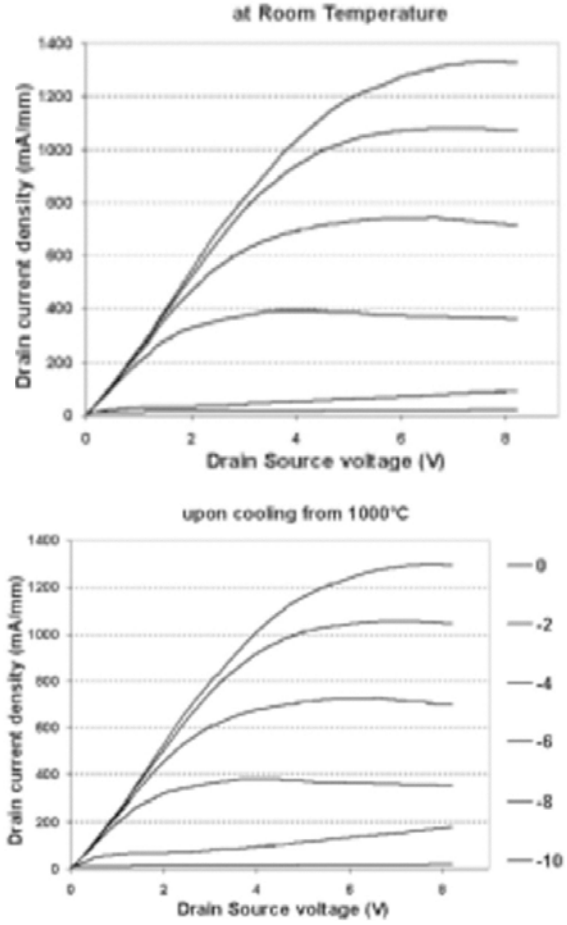

Fig. (15). Output characteristics of the HEMT device before and after the temperature cycling test up to 1000 °C.

Unlike AlGaN/GaN devices, where contacts have been stable up to the highest temperature of operation (800 °C [26]), but the 2DEG density and maximum channel current density have started to degrade first, the lattice matched InAlN/GaN heterostructure appears to be extremely stable. No degradation of the polarization fields in the two materials, the heterojunction or the 2DEG density is observed. Recent materials studies have indeed confirmed the outstanding thermal stability of the InAlN/GaN heterostructure [27].

CONCLUSIONS

The significant advancements achieved in the InAlN/GaN heterostructure growth techniques by MOCVD have enabled to demonstrate the expected high sheet carrier density together with high mobilities. These material properties have indeed resulted in record device characteristics. However, the process technology is still immature; in particular an efficient surface passivation scheme has still to be developed in order to stabilize the surface and remove the residual surface trapping. First small signal characteristics show that the AlGaN/GaN HEMT scaling limit can be overcome and ultra short gate lengths (lower than 50 nm) may be possible while keeping a high aspect ratio in conjunction with a high sheet carrier density. Thus the system promises very high power densities at high frequency and Enhancement-Mode of operation in a planar configuration.

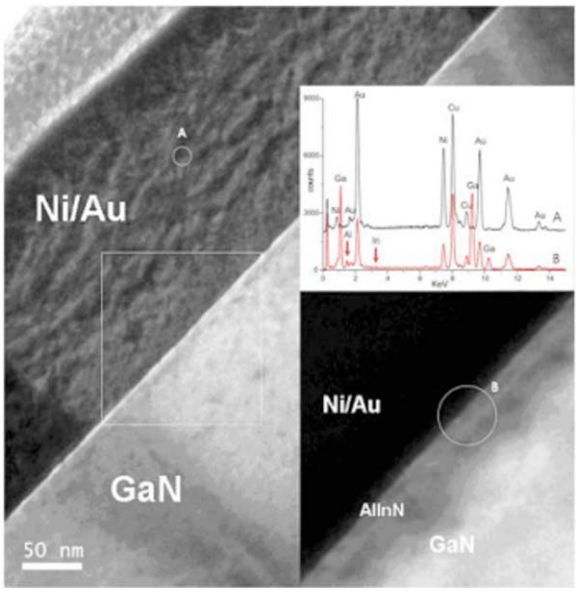

Fig. (16). HR-TEM image of the interface between the Ni/Au Schottky contact and the InAlN/GaN heterostructure upon cooling from 1000°C. The insert in this figure shows the EDX spectrum recorded in the Ni/Au alloy (zone A) and in the InAlN barrier layer (zone B). Copper (Cu) and Ga peaks come from the grid and from FIB (Focused Ion Beam) preparation, respectively.

In the lattice matched composition the materials system is chemically extremely stable. This has allowed FET operation at 1000 °C in vacuum for the first time. In this first short time experiment it could be seen that neither the ohmic contacts, nor the Schottky contacts or the heterostructure itself had degraded. This may eventually translate into high reliability and robustness under very high power operation.

With the aim of reaching the highest 2DEG channel sheet charge concentration of the III-Nitride system, the reduction of the In content in the InAlN barrier layer while maintaining high mobility will still be an attractive growth challenge for the future.

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