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# Variable Length Reconfigurable Algorithms and Architectures for DCT/IDCT Based on Modified Unfolded Cordic

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**Abstract:** A coordinate rotation digital computer (CORDIC) based variable length reconfigurable DCT/IDCT algorithm and corresponding architecture are proposed. The proposed algorithm is easily to extend to the $2^n$-point DCT/IDCT. Furthermore, we can easily construct the N-point DCT/IDCT with two N/2-pt DCTs/IDCTs based the proposed algorithm. The architecture based on the proposed algorithm can support several power-of-two transform sizes. To speed up the computation of DCT/IDCT without losing accuracy, we develop the modified unfolded CORDIC with the efficient carry save adder (CSA). The rotation angles of CORDIC used in proposed algorithm are arithmetic sequence. For convenience, we develop the architecture of N-point IDCT with the orthogonal property of DCT and IDCT transforms. The proposed architecture are modeled with MATLAB language and performed in DCT-based JPEG process, the experimental results show that the peak signal to noise ratio (PSNR) values of proposed architectures are higher than the existing CORDIC based architectures at both different quantization factors and different test images. Furthermore, the proposed architectures have higher regularity, modularity, computation accuracy and suitable for VLSI implementation.

**Keywords:** DCT/IDCT, CORDIC, variable length reconfigurable, carry save adder.

## 1. INTRODUCTION

The discrete cosine transform (DCT) and its inverse (IDCT) [1] are the most widely used transforms in the image and signal processing due to the near optimal performance for compression of a highly correlated data. The commonly used DCT algorithms aim at speeding up the computation [2-4], or reducing the complexity of the architecture and computation [5, 6]. Loeffler based architectures [7-9] use the flow-graph algorithm to reduce computation complexity and make computation more efficiently. However, current existing algorithms often suffer from a lack of scalability and hardly to be extended to the variable length DCT/IDCT. With the development of signal processing systems, variable length reconfigurable architectures for DCT/IDCT are highly desirable for low power applications, multi-standard, and multi-mode environments. Some reconfigurable DCT/IDCT architectures [10-12] are proposed in the literature. However, all of them have their drawbacks, such as changing different reconfigurable modules [10] or different pre-processing and post-processing stages [12] to realize different processor, using a greedy algorithm [11]. Furthermore, they do not have the scalability to adapt to power-of-tow transform size.

CORDIC-based architectures are suitable for VLSI implementation with regularity and simple hardware architecture. However, due to the recursive nature of itself, it is difficult to realize pipeline [12]. Using the unfolding technique can overcome this problem [13-15], but will introduce new problems, such as numerical inaccuracy, the scalability problem of variable length DCT computations.

In this paper, we propose a computationally efficient and variable length reconfigurable DCT/IDCT algorithm and corresponding architecture. Based on the proposed algorithm, we can easily obtain the $2^n$-point DCT/IDCT and construct the N-point DCT/IDCT with two N/2-point DCTs/IDCTs. The proposed architecture of one-dimension (1-D) 8-point DCT is developed, and the architecture of 1-D 8-point IDCT is developed by taking the orthogonal property of DCT and IDCT transforms. To enhance the computation accuracy of the unfolded CORDIC and improve the performance, a modified unfolded CORDIC is proposed. The modified unfolded CORDIC has better accuracy than conventional ones as well as computation efficiency by taking advantage of its certain property of using carry save adders (CSAs). Furthermore, based on the row-column decomposition algorithm, the 2-D 8×8 DCT/IDCT architecture with the modified unfolded CORDIC is implemented and verified in DCT-based JPEG process model. The experimental results show that the proposed architectures have the good transformation quality compared to the existing CORDIC based DCT in terms of PSNR results.

The paper is organized as follows. In section 2, we derive the variable length reconfigurable DCT/IDCT algorithm based on the CORDIC. In section 3, the signal flows of the proposed algorithm are depicted in detail. In section 4, the architectures design of the 4/8-point DCT/IDCT based on modified unfolded CORDIC are presented. The experimental results and conclusion can be found in section 5 and 6.

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## 2. PROPOSED VARIABLE LENGTH RECONFIGURABLE DCT/ IDCT ALGORITHM

For a N-point signal, $x[n]$, the type-II DCT and IDCT are defined as [6]:

$$C[k]=\alpha[k]\sum_{n=0}^{N-1}x[n]\cos\left[\frac{(2n+1)k\pi}{2N}\right],(k=0,....,N-1) \quad (1)$$

$$x[n]=\sum_{k=0}^{N-1}\alpha[k]C[k]\cos\left[\frac{(2n+1)k\pi}{2N}\right],(n=0,....,N-1) \quad (2)$$

where $\alpha[0]=1/\sqrt{N}$, and $\alpha[k]=\sqrt{2/N}$ for $k>0$.

The type-II discrete sine transform (DST) is defined as:

$$S[k]=\alpha[k]\sum_{n=0}^{N-1}x[n]\sin\left[\frac{(2n+1)k\pi}{2N}\right],k=1,....,N \quad (3)$$

where $\alpha[N]=1/\sqrt{N}$, and $\alpha[k]=\sqrt{2/N}$ for $k<N$.

According to (1) and (3), neglecting the post-scaling factor without loss generality, the main operation of an N-point DCT and DST denoted as $\widetilde{\mathrm{DCT}}$ and $\widetilde{\mathrm{DST}}$ can be written as:

$$\widetilde{C}[k]=\sum_{n=0}^{N-1}x[n]\cos\left[\frac{(2n+1)k\pi}{2N}\right],k=0,\cdots,N-1 \quad (4)$$

$$\widetilde{S}[k]=\sum_{n=0}^{N-1}x[n]\sin\left[\frac{(2n+1)k\pi}{2N}\right],k=1,\cdots,N \quad (5)$$

A length-N input sequence $x[n]$, with N being power of two, can be decomposed into $x_L[n]$ and $x_H[n]$, which denote the low-frequency and high-frequency sub-band signals of $x[n]$ respectively [16], are defined as:

$$x_L[n]=\frac{1}{2}\{x[2n]+x[2n+1]\} \quad (6)$$

$$x_H[n]=\frac{1}{2}\{x[2n]-x[2n+1]\} \quad (7)$$

where $n=0,1,2,....,(N/2)-1$

Thus, the original signal $x[n]$ can be obtained from $x_L[n]$ and $x_H[n]$ as follows:

$$x[2n]=x_L[n]+x_H[n] \quad (8)$$

$$x[2n+1]=x_L[n]-x_H[n] \quad (9)$$

Substituting (8) and (9) into (4), (4) can be rewritten as:

$$\begin{aligned}\widetilde{C}[k]=&\sum_{n=0}^{(N/2)-1}x[2n]\cos(\frac{(4n+1)k\pi}{2N})\\&+\sum_{n=0}^{(N/2)-1}x[2n+1]\cos(\frac{(4n+3)k\pi}{2N})\\&=2\cos(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}x_L[n]\cos(\frac{(2n+1)k\pi}{N})\\&+2\sin(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}x_H[n]\sin(\frac{(2n+1)k\pi}{N})\end{aligned} \quad (10)$$

where $k=0,....,N-1$.

Since

$$\begin{aligned}\cos\left[\frac{(2n+1)(N/2-l)\pi}{N}\right]=&\cos(\frac{2n+1}{2}\pi)\cos(\frac{2n+1}{N}l\pi)\\&+\sin(\frac{2n+1}{2}\pi)\sin(\frac{2n+1}{N}l\pi)\\=&\sin(\frac{2n+1}{2}\pi)\sin(\frac{2n+1}{N}l\pi)\end{aligned} \quad (11)$$

We get

$$\sin(\frac{2n+1}{N}l\pi)=(-1)^n\cos\left[\frac{(2n+1)(N/2-l)\pi}{N}\right] \quad (12)$$

Let

$$\hat{x}_H[n]=(-1)^n x_H[n] \quad (13)$$

According to (12) and (13), (10) can be rewritten as:

$$\tilde{C}(k)=\begin{cases}2\cos(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}x_L[n]\cos\left[\frac{(2n+1)k\pi}{N}\right]\\+2\sin(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}\hat{x}_H[n]\cos\left[\frac{(2n+1)(N/2-k)\pi}{N}\right]\\,k=0,\cdots,N/2-1\\2\cos(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}x_L[n]\cos\left[\frac{(2n+1)k\pi}{N}\right]\\+2\sin(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}\hat{x}_H[n]\cos\left[\frac{(2n+1)(N/2-k)\pi}{N}\right]\\,k=N/2,\cdots N-1\end{cases} \quad (14)$$

Let $l=N-k$, we get

$$\tilde{C}(k)=\begin{cases}2\cos(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}x_L[n]\cos\left[\frac{(2n+1)k\pi}{N}\right]\\+2\sin(\frac{\pi k}{2N})\sum_{n=0}^{(N/2)-1}\hat{x}_H[n]\cos\left[\frac{(2n+1)(N/2-k)\pi}{N}\right]\\,k=0,\cdots,N/2-1\\-2\sin(\frac{\pi l}{2N})\sum_{n=0}^{(N/2)-1}x_L[n]\cos\left[\frac{(2n+1)l\pi}{N}\right]\\+2\cos(\frac{\pi l}{2N})\sum_{n=0}^{(N/2)-1}\hat{x}_H[n]\cos\left[\frac{(2n+1)(N/2-l)\pi}{N}\right]\\,l=1,\cdots,N/2,k=N/2,\cdots N-1\end{cases} \quad (15)$$

In (15), except $k=0,N/2$ all the points can be evaluated by (N/2)-point $\widetilde{\mathrm{DCT}}$. Therefore, we separate the formula (15) into four parts shown as:

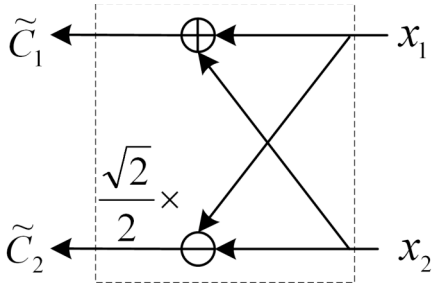



**Fig. (1).** Signal flow graph of the 2-point DCT.

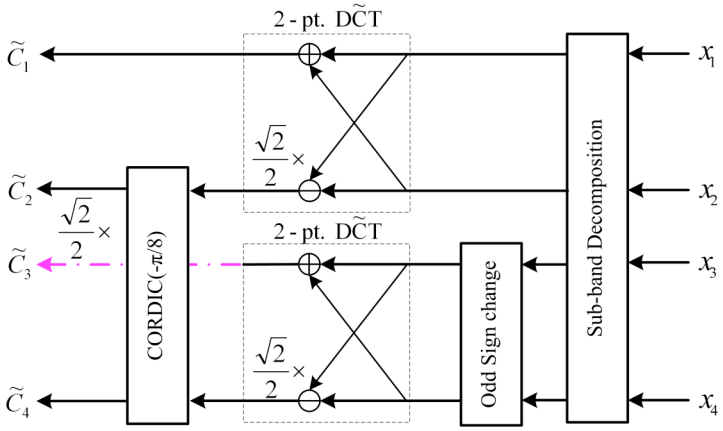



**Fig. (2).** Signal flow graph of the 4-point DCT.

$$\tilde{C}(0) = 2\sum_{n=0}^{(N/2)-1} x_L[n]$$

$$\tilde{C}(N/2) = \sqrt{2}\sum_{n=0}^{(N/2)-1} (-1)^n x_H[n]$$

$$\begin{bmatrix} \tilde{C}(k) \\ \tilde{C}(N-k) \end{bmatrix} = 2\begin{bmatrix} \cos(\frac{k\pi}{2N}) & \sin(\frac{k\pi}{2N}) \\ -\sin(\frac{k\pi}{2N}) & \cos(\frac{k\pi}{2N}) \end{bmatrix} \cdot \begin{bmatrix} \tilde{C}_L(k) \\ \tilde{C}_{\hat{H}}(N/2-k) \end{bmatrix}, k = 1, \cdots, N/2-1 \quad (16)$$

Where $\widetilde{C}_L$ and $\widetilde{C}_{\hat{H}}$ denoting the (N/2)-point $\widetilde{\text{DCT}}$ of the $x_L(n)$ and $\hat{x}_H(n)$ respectively.

As one can see, we can evaluate the N-point $\widetilde{\text{DCT}}$ with two (N/2)-point $\widetilde{\text{DCT}}$s based on the CORDIC algorithm. Therefore, the proposed algorithm is a variable length reconfigurable algorithm for DCT, and easily extended to $2^n$-point DCT. In addition, the rotation angles of the CORDICs are arithmetic sequence which has a common difference of $\frac{-\partial}{2N}$, from $\frac{-\partial}{2N}$ to $\frac{-(N/2-1)\partial}{2N}$. Similarly, the variable length reconfigurable algorithm of the N-point IDCT can be deduced. Alternatively, the orthogonal property of DCT and IDCT transforms can be used to obtain the reconfigurable algorithm for the N-point IDCT more easily, which will be depicted in detail in section III.

## 3. SIGNAL FLOW OF THE PROPOSED DCT/IDCT ALGORITHM

In this section, we depict the variable length reconfigurable DCT/IDCT signal flows based on the proposed algorithm in detail.

According to (4), 2-point $\widetilde{\text{DCT}}$ computation is as follows

$$\begin{bmatrix} \tilde{C}_1 \\ \tilde{C}_2 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ \frac{\sqrt{2}}{2} & -\frac{\sqrt{2}}{2} \end{bmatrix} \cdot \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \quad (17)$$

Thus, the signal flow graph of computing the 2-point $\widetilde{\text{DCT}}$ can be depicted as Fig. (**1**).

According to (16), the signal flow graph of computing the 4-point $\widetilde{\text{DCT}}$ can be constructed by two 2-point $\widetilde{\text{DCT}}$s, which depicted as Fig. (**2**).

According to (6) and (7), the sub-band decomposition matrix is shown as:

$$D_4 = \begin{bmatrix} 1 & 1 & & \\ & & 1 & 1 \\ 1 & -1 & & \\ & & 1 & -1 \end{bmatrix} \quad (18)$$

According to (13) the odd sign change matrix is shown as:

$$s_2 = \begin{bmatrix} 1 & \\ & -1 \end{bmatrix} \quad (19)$$

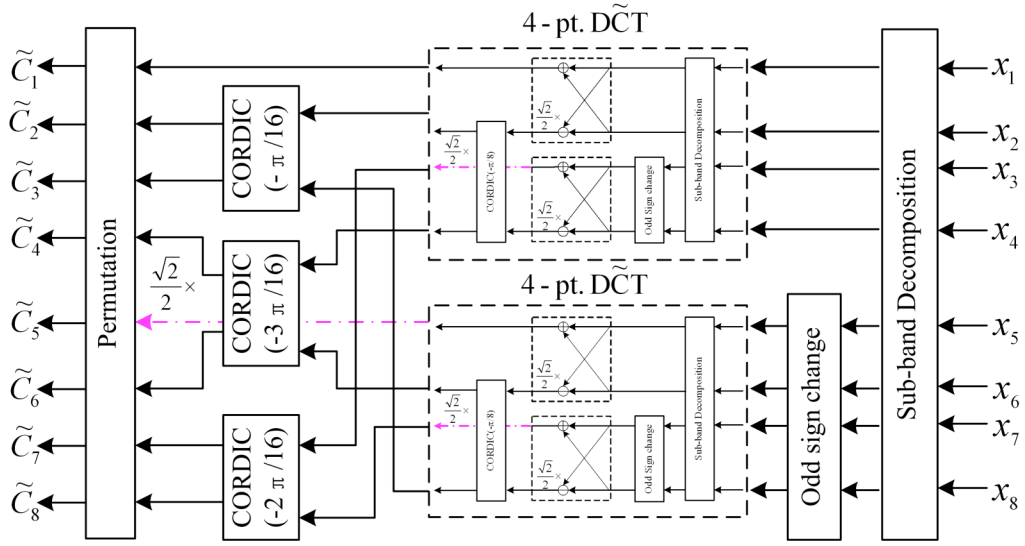



**Fig. (3).** Signal flow graph of the 8-point DCT.

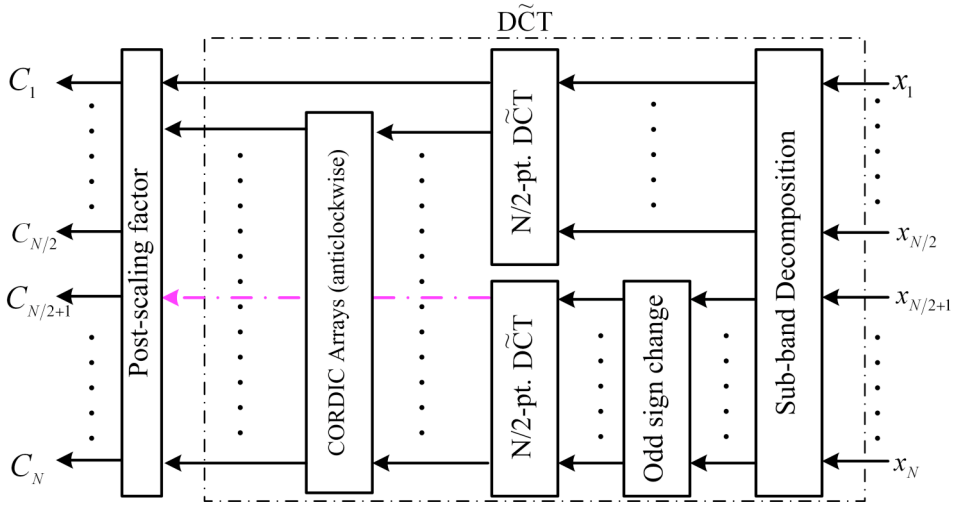



**Fig. (4).** Signal flow graph of the N-point DCT.

Similarly, the signal flow graph of computing the 8-point DCT can be constructed by two 4-point DCTs, which depicted as Fig. (**3**).

In Fig. (**3**) the 4-point DCTs are bordered by the dashed lines and the sub-band decomposition matrix is shown as:

$$D_8 = \begin{bmatrix} 1 & 1 & & & & & & \\ & & 1 & 1 & & & & \\ & & & & 1 & 1 & & \\ & & & & & & 1 & 1 \\ 1 & -1 & & & & & & \\ & & 1 & -1 & & & & \\ & & & & 1 & -1 & & \\ & & & & & & 1 & -1 \end{bmatrix} \quad (20)$$

The odd sign change matrix of 8-point DCT is shown as:

$$s_4 = \begin{bmatrix} 1 & & & \\ & -1 & & \\ & & 1 & \\ & & & -1 \end{bmatrix} \quad (21)$$

As described above, according to (1) and (16), the signal flow graph of computing the N-point DCT with two N/2-point DCTs can be generalized, which depicted as Fig. (**4**).

In Fig. (**4**) the N-point DCTs are bordered by dash lines, and the post-scaling factor of N-point DCT is $\alpha_N = \left[ \frac{1}{\sqrt{N}} \ , \sqrt{\frac{2}{N}} \ , \cdots \ \sqrt{\frac{2}{N}} \right]_N$. According to (16), the CORDIC arrays contain (N/2-1) CORDIC cell with the rotation angles from $\frac{-\partial}{2N}$ to $\frac{-(N/2-1)\partial}{2N}$.

The sub-band decomposition matrix of the N-point DCT is shown as:

$$D_N = \begin{bmatrix} 1 & 1 & & & & \\ & \ddots & \ddots & & & \\ & & & 1 & 1 & \\ 1 & -1 & & & & \\ & \ddots & \ddots & & & \\ & & & 1 & -1 & \end{bmatrix}_N \quad (22)$$

**Table 1. Transfer Functions of DCT and IDCT**

| Symbol | DCT | IDCT |
|---|---|---|
| Butterfly | $x_{out} = x_{in} + y_{in}$<br>$y_{out} = x_{in} - y_{in}$ | $x_{out} = (x_{in} + y_{in})/2$<br>$y_{out} = (x_{in} - y_{in})/2$ |
| Multiply constant | $\xleftarrow{K\times}$ | $\xrightarrow{\times\frac{1}{K}}$ |
| CORDIC | Clockwise (-θ) | Anticlockwise (θ) |

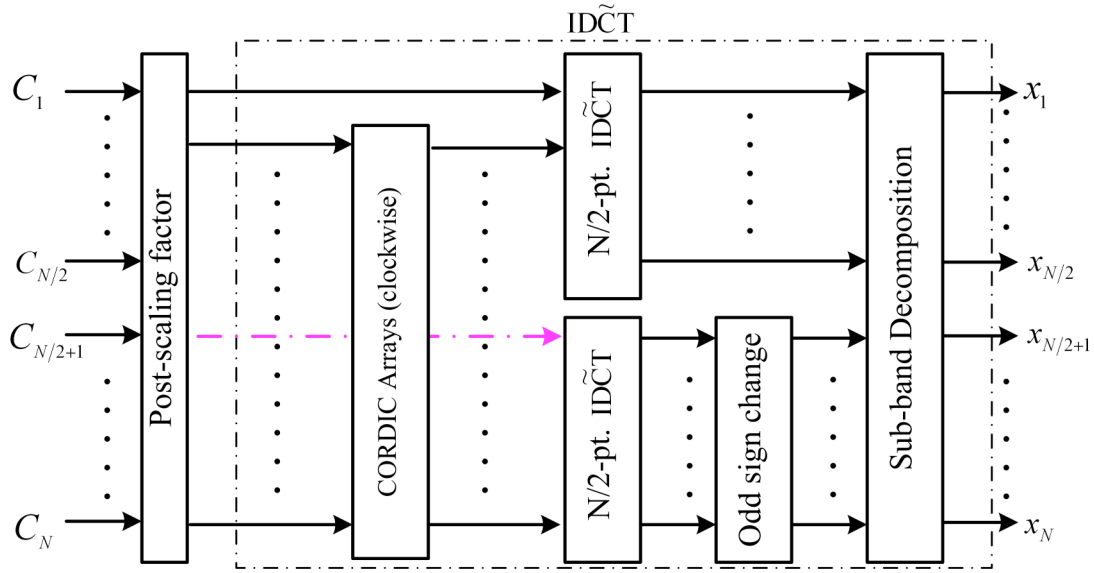



**Fig. (5).** Signal flow graph of the N-point IDCT.

The odd sign change matrix of the N-point DCT is shown as:

$$s_{N/2} = \begin{bmatrix} 1 & & & \\ & -1 & & \\ & & \ddots & \\ & & & -1 \end{bmatrix}_{N/2} \tag{23}$$

The N-point DCT can be obtained by multiply N-point $\widetilde{\text{DCT}}$ by the post-scaling factor, and permuted according to (16). Furthermore, we can combine the constant value $\sqrt{2}/2$ in signal flow graph with the post-scaling factor, thus we have unified post-scaling factor $1/\sqrt{N}$ for all outputs. For 2-D DCT, we can deal the two 1-D DCT post-scaling factors together by multiplying the constant value $1/N$. As Fig. (**4**) depicts, the first N/2-point $\widetilde{\text{DCT}}$ transform is executed by the upper part of the flow graph and the second N/2-point $\widetilde{\text{DCT}}$ transform is executed by the lower part. Thus, the architecture based on this signal flow can be used to compute N-point, as well as N/2-point, N/4-point, …, 2-pointDCT/IDCT by only changing the positions of the inputs and outputs. Additionally the post-scaling factors should be taken under consideration.

According to (1) and (2), DCT and IDCT are orthogonal transforms, the signal flow of the N-point IDCT can be easily obtained by inverting the transfer functions of each building block shown in Table **1** and reversing the signal flow direction [17, 18]. Fig. (**5**) depicts the signal flow of the N-point IDCT.

## 4. ARCHITECTURE DESIGN FOR THE RECONFIGURABLE 4/8-POINT DCT/IDCT BASED ON MODIFIED UNFOLDED CORDIC

Without loss the generality, based on the proposed variable length reconfigurable DCT/IDCT algorithm, we develop an efficient 4/8-point DCT/IDCT architecture in this section. A modified unfolded CORDIC architecture is proposed to improve the performance and reduce the hardware complexity.

In the CORDIC algorithm, to rotate a vector (x, y) by an angle θ, the circular rotation angle is decomposed as:

$$\theta = \sum_i \sigma_i \cdot \tan^{-1}(2^{-i}), \text{ where } \sigma_i = \pm 1 \tag{24}$$

Then, the vector rotation can be performed iteratively as follow [10, 13, 15]:

$$\begin{aligned} x_{i+1} &= x_i - \sigma_i \cdot y_i \cdot 2^{-i} \\ y_{i+1} &= y_i + \sigma_i \cdot x_i \cdot 2^{-i} \end{aligned} \tag{25}$$

**Table 2. Used Rotation Angle and Compensation**

| Angle | -π/16 | -π/8 | -3π/16 |
|---|---|---|---|
| Rotation iterations [ $\sigma_i, i$ ] according to (25) | | | |
| 1 | -1,3 | -1,2 | -1,1 |
| 2 | -1,4 | -1,3 | -1,3 |
| 3 | -1,7 | -1,6 | -1,10 |
| 4 | -1,9 | -1,7 | -1,14 |
| Compensation iterations [ $(1+\gamma_i \cdot F_i)$ ] according to (27) | | | |
| 1 | 1-1/128 | 1-1/32 | 1-1/8 |
| 2 | 1-1/512 | 1-1/128 | 1+1/64 |
| 3 | | 1+1/1024 | 1+1/1024 |
| 4 | | 1+1/4096 | 1+1/4096 |

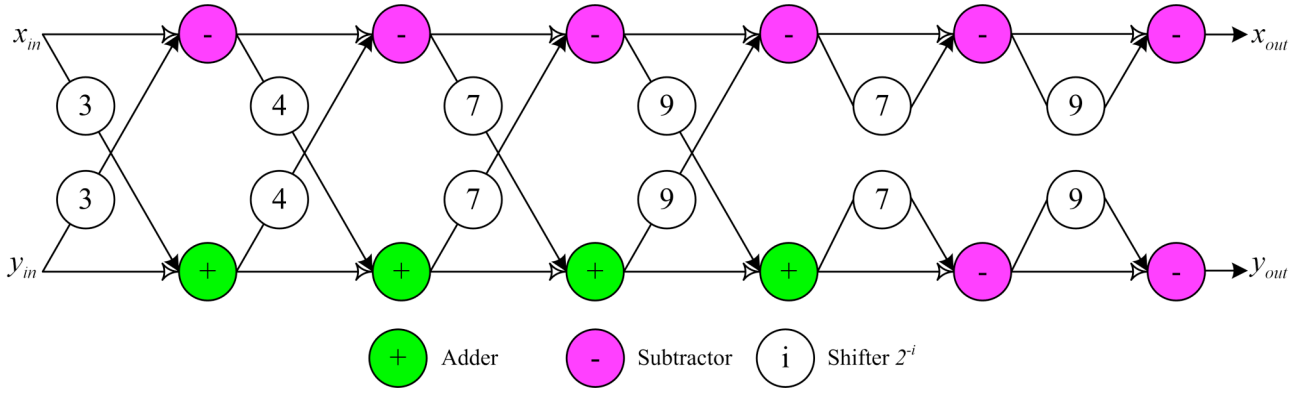



**Fig. (6).** Unfolded CORDIC flow graph of the -π/16.

Furthermore, the results of the rotation iterations need to be scaled by a compensation factor s.

$$s = \prod_i (\cos(\arctan(2^{-i}))) \tag{26}$$

Alternatively, replacing (26) with the following iterative method.

$$\begin{aligned} x_{i+1} &= x_i(1+\gamma_i \cdot F_i) \\ y_{i+1} &= y_i(1+\gamma_i \cdot F_i) \end{aligned} \tag{27}$$

Where $\prod_i (1+\gamma_i \cdot F_i) \cong s, \gamma_i = (0,1,-1), F_i = 2^{-i}$

In (25) and (27), only shift and add operations are required to perform the operation.

Since rotation angles of CORDICs are fixed in the proposed DCT/IDCT algorithm, we can skip some unnecessary CORDIC iterations. According to (16), for 8-point DCT, three different fixed angles are needed to rotate. The number and compensation of iterations are given in Table **2**.

According to Table **2**, the unfolded CORDIC flow graph of the -π/16 angle is shown as Fig. (**6**).

In Fig. (**6**), it needs six shifts and six additions operations to evaluate the -π/16 angle rotation. To evaluate the rotation more efficiently without losing accuracy, when the sequence iterations numbers $i$ and $j$ are big enough, two iterations can be combined into one iteration according to the equations as follow:

$$\begin{aligned} x_{k+i+j} &= x_k - \sigma_i \cdot y_k \cdot 2^{-i} - \sigma_j \cdot y_k \cdot 2^{-j} - \sigma_i\sigma_j \cdot x_k \cdot 2^{-(i+j)} \\ &\cong x_k - \sigma_i \cdot y_k \cdot 2^{-i} - \sigma_j \cdot y_k \cdot 2^{-j} \\ y_{k+i+j} &= y_k + \sigma_i \cdot x_k \cdot 2^{-i} + \sigma_j \cdot x_k \cdot 2^{-j} - \sigma_i\sigma_j \cdot y_k \cdot 2^{-(i+j)} \\ &\cong y_k + \sigma_i \cdot x_k \cdot 2^{-i} + \sigma_j \cdot x_k \cdot 2^{-j} \end{aligned} \tag{28}$$

Similarly, (27) can be approximated as follow:

$$\begin{aligned} x_{i+j+1} &= x_i(1+\gamma_i \cdot F_i + \gamma_j \cdot F_j + \gamma_i\gamma_j \cdot F_i) \\ &\cong x_i(1+\gamma_i \cdot F_i + \gamma_j \cdot F_j) \\ y_{i+j+1} &= y_i(1+\gamma_i \cdot F_i + \gamma_j \cdot F_j + \gamma_i\gamma_j \cdot F_i) \\ &\cong y_i(1+\gamma_i \cdot F_i + \gamma_j \cdot F_j) \end{aligned} \tag{29}$$

where $\gamma_{i,j} = (0,1,-1), F_{i,j} = 2^{-i,j}$

According to (28) and (29), we obtain the modified unfolded CORDIC. The modified unfolded CORDIC needs less shift and add operations without losing accuracy under certain condition. The modified unfolded CORDIC flow graph of the -π/16 is shown in Fig. (**7**). In order to gain higher accuracy, the shift numbers are optimized by numerical simulation in MATLAB, and a subtle change (7 to 6) is made in third shift stage.

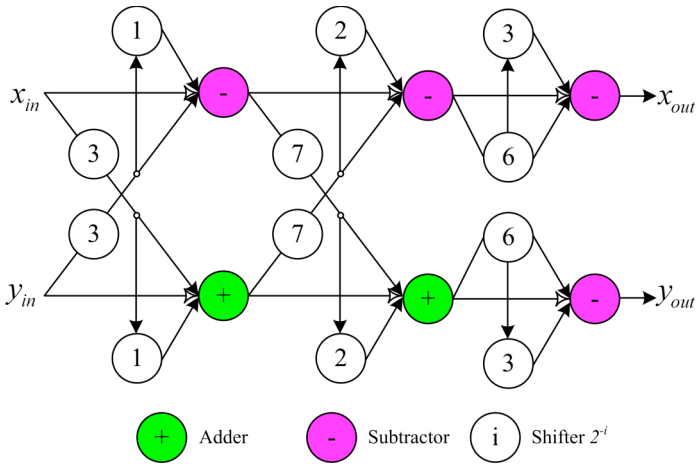
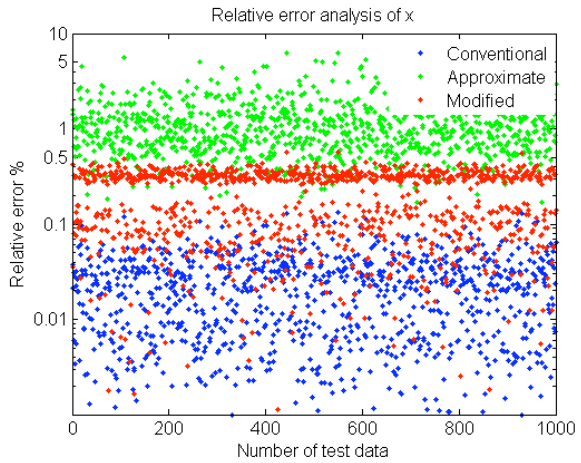
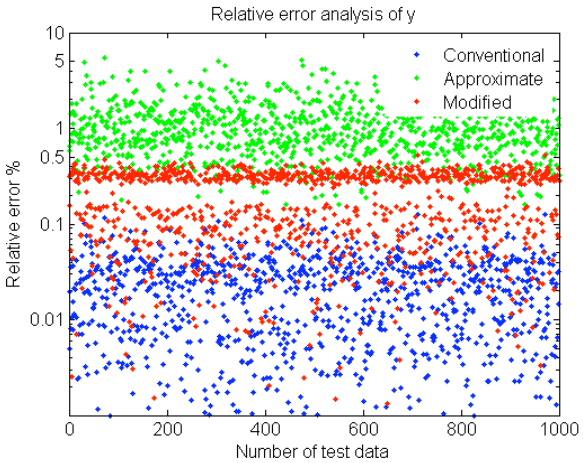



**Fig. (7).** Modified unfolded CORDIC flow graph of the -π/16.




(**a**)




(**b**)

**Fig. (8).** Relative errors of the three CORDICs with -π/16 rotation angle.

In Fig. (**7**), as one can see, it needs three shifts and three additions to evaluate the -π/16 angle rotation. Furthermore, we can implement the CORDIC architecture with more efficient adder CSAs, which make the computation faster.

To evaluate the accuracy of the modified unfolded CORDIC, we take two types unfolded CORDIC as references. One is the conventional unfolded CORDIC which meets the precision requirements of IEEE Std. 1180-1990 [15], the other one is an approximate unfolded CORDIC [9]. The word-length of inputs and outputs are both 12-bits, and the test data are 1000 uniform random data. The computation relative errors of the three CORDICs are evaluated, and the compared results of the two outputs (x, y) of the CORDIC are shown as Fig. (**8**).

In Fig. (**8**), it can be seen that the computation results of the modified unfolded CORDIC have much smaller relative

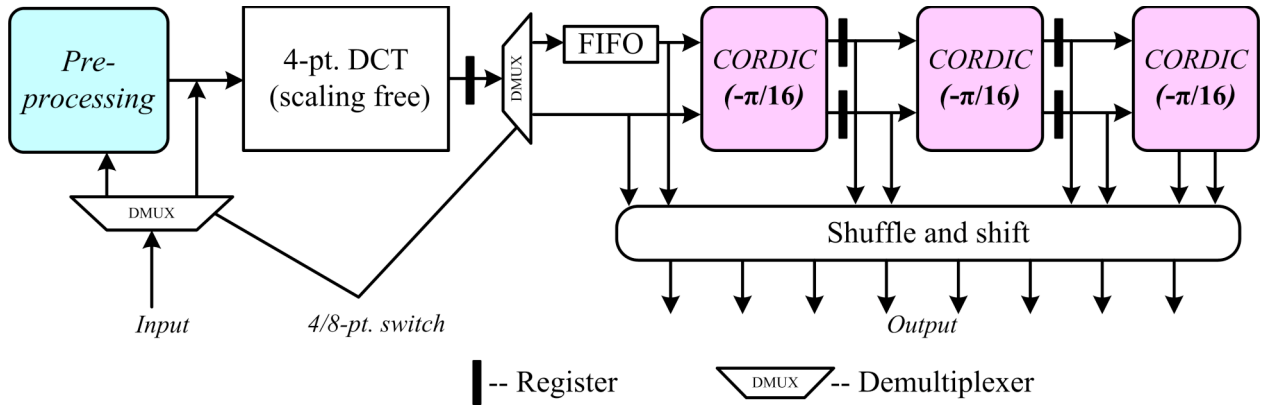



**Fig. (9).** The reconfigurable 4/8-point DCT architecture based on the modified unfolded CORDIC.

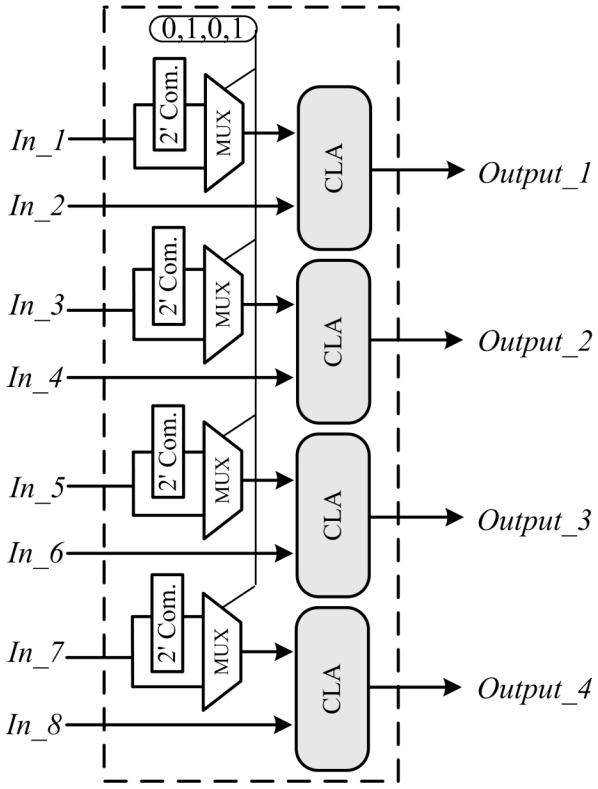



**Fig. (10).** The architecture of the pre-processing element.

error than the approximate unfolded CORDIC [9], and nearly the same values as the conventional unfolded CORDIC. In addition, most of relative error values of the modified unfolded CORDIC are under 0.4%.

Since the iteration numbers of the $-\pi/8$ and $-3\pi/16$ are not meet the accuracy requirements, if directly using the formula (28) and (29), the double angle formula is used alternatively. According to the double angle formula, the operation of rotating $2\theta$ can be replaced by two sequential operations of rotating $\theta$, and three sequential operations of rotating $\theta$ for $3\theta$. Moreover, the computation accuracy of the $-\pi/8$ and $-3\pi/16$ architectures can meet the requirements in most signal processing application, such as JPEG, which will be verified in section 5.

We take a reconfigurable 4/8 DCT architecture as an example to implement the proposed algorithm. According to the Fig. (**3**), we separate the signal flow into two parts: the upper 4-point DCT and the lower 4-point DCT. Since the two 4-point DCTs are independent, we can reuse the 4-point DCT processor and implement the reconfigurable 4/8-pointDCT architecture in series manner, which depicts as Fig. (**9**). Furthermore, we can implement the three rotations with only three same CORDIC processors, thus the proposed architecture has high reusability and modularity. Comparing with the existing reconfigurable architecture, our architecture no need to change any architecture to switch from 4-point to 8-point DCT processor, and is suitable for VLSI implementation.

In Fig. (**9**), we use the demultiplexer to dynamically switch from 4-point to 8-point DCT without changing the architecture. The FIFO is used to store the immediate results generated by the 4-point DCT that implemented with two $-\pi/16$ CORDIC processors. The architecture of the pre-processing element is shown as Fig. (**10**).

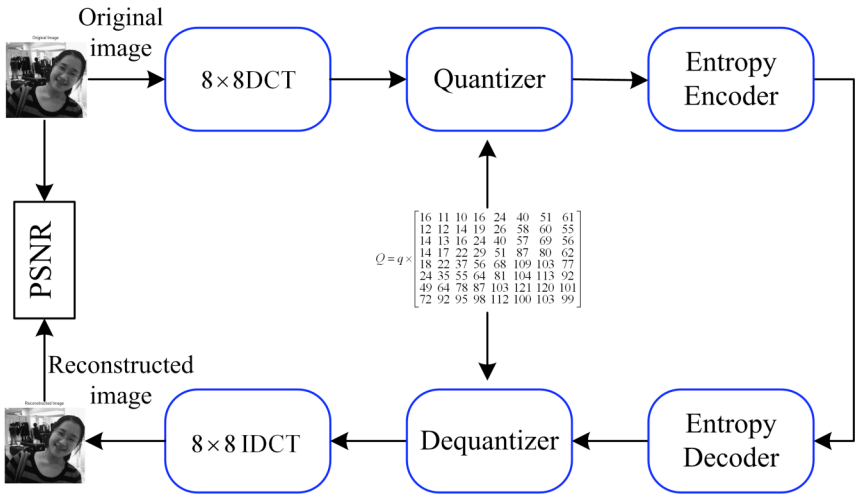



**Fig. (11).** Block diagram of DCT based JPEG process.

**Table 3. PSNR and CR at Different Quantization Factors *q* (Board)**

| *q* | PSNR (dB) | | | CR | | |
|---|---|---|---|---|---|---|
| | [9] | [15] | Proposed | [9] | [15] | Proposed |
| 0.1 | 41.76 | 41.82 | 42.27 | 1.22 | 1.22 | 1.22 |
| 0.3 | 33.06 | 33.06 | 33.13 | 1.84 | 1.85 | 1.84 |
| 0.5 | 29.26 | 29.26 | 29.30 | 2.31 | 2.33 | 2.32 |
| 1 | 25.02 | 25.02 | 25.04 | 3.32 | 3.34 | 3.33 |
| 3 | 20.24 | 20.24 | 20.25 | 6.31 | 6.34 | 6.33 |
| 5 | 18.36 | 18.36 | 18.37 | 8.66 | 8.70 | 8.70 |
| 10 | 16.06 | 16.06 | 16.06 | 14.05 | 14.16 | 14.15 |

In Fig. (**10**), we use 2' complement to implement the subtract operation and use multiplexer (MUX) to chose add operation or subtract operation.

We use the transposing property depicted in Table **1** to implement the 4/8-point reconfigurable IDCT architecture. When change CORDIC from clockwise rotation to anti-clockwise rotation with same angle, the only thing need to do is change the sign of $\sigma_i$, or equivalently change all adders to subtractors, and subtractors to adders respectively in rotation iterations stage.

## 5. EXPERIMENTAL RESULTS

To verify the performance of the proposed architecture, we design and estimate three different architectures: Loeffler [9], Jeong [15], and the proposed architecture with 12-bit accuracy using MATLAB language. After modeling the four architectures, we use the DCT-based JPGE process model to verify their performance. Fig. (**11**) depicts the block diagram of DCT-based JPGE process model. The architecture of $8\times8$ 2-D DCT/IDCT is implemented using two cascading 1-D DCT/IDCT architectures with one transpose memory [16]. In this paper, we use the peak signal-to-noise ratio (PSNR) to measure the reconstructed image quality. The values of PSNR are measured by sending image data through the JPGE process including the DCT architecture and IDCT architecture.

The quantization factor $q$ is used to trade off image quality and compression ratio (CR). Huffman coding is used as entropy code, and the quantization matrix in Fig. (**11**), as specified in the original JPEG standard, is as follows:

$$Q = q\times\begin{bmatrix} 16 & 11 & 10 & 16 & 24 & 40 & 51 & 61 \\ 12 & 12 & 14 & 19 & 26 & 58 & 60 & 55 \\ 14 & 13 & 16 & 24 & 40 & 57 & 69 & 56 \\ 14 & 17 & 22 & 29 & 51 & 87 & 80 & 62 \\ 18 & 22 & 37 & 56 & 68 & 109 & 103 & 77 \\ 24 & 35 & 55 & 64 & 81 & 104 & 113 & 92 \\ 49 & 64 & 78 & 87 & 103 & 121 & 120 & 101 \\ 72 & 92 & 95 & 98 & 112 & 100 & 103 & 99 \end{bmatrix} \quad (30)$$

Firstly, we use the scale gray image 'Board' of size 256 × 256 as test image. The values of PSNR and CR of the three different DCT/IDCT architectures are calculated at different quantization factor $q$, and the compared results are presented in the Table **3**.

From the Table **3**, one may observe that the PSNR values of the proposed DCT architecture are better than the other DCT architectures at most of the different values of $q$. In addition, the CR values of the proposed architecture are better than the architectures of Loeffler [9] and Matrix multiplication at all different values of $q$, and nearly the same values


**Fig. (12).** Reconstructed image from different algorithm of DCT at $q = 1$.

as the architecture of Jeong [15]. This implies that the proposed architecture not only makes the computation faster, since using the modified unfolded CORDIC architecture, but also improves the quality of the results in terms of PSNR values.

Experimentations have been also carried out with four well-known grey scale test images, the image of 'Lena', 'Baboon', 'Peppers', 'Board' of size 256 × 256, with quantization factor $q = 1$. The original images and reconstructed images with PSNR values are demonstrated in Fig. (**12**).

## 6. CONCLUSION

In this paper, we derive a variable length reconfigurable DCT/IDCT algorithm, and develop the reconfigurable 4/8-point DCT architecture based on modified unfolded CORDIC. Specifically, the rotation angles used in our proposed

architecture are arithmetic sequence. Consequently, we can use double angle formula to implement the bigger angle rotation with the smaller angle rotation, which make the architecture has higher modularity. In addition, it has higher computation accuracy than the existing architectures [9, 15], and higher regularity and modularity than the existing architectures [10-12]. The future work includes VLSI implementation for the proposed architecture using systolic arrays, the applications on data dependent compression using the proposed architecture.

## CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

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