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Implementation of a Data Acquisition System for 2×2 Fiber Optic Taper Array Coupled Digital X-ray Detector

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Abstract: Fiber optic taper (FOP) array coupled digital x-ray detector can be an ideal choice for large area high resolution x-ray imaging, but its data acquisition system is a challenge, for the reasons such as restrictions of hardware design due to the shape of the FOP array, long distance control requirement in x-ray environment, and arrangement of data transmission sequence among multiple CCD/CMOS image sensors. A FPGA and ARM based data acquisition system for 2×2 FOP array coupled x-ray detector was implemented in this paper. We have finished all the procedures involving the data acquisition system, including hardware and PCB design, FPGA design, ARM and PC software development, and so on. The data acquisition process operates in parallel during parameters setting, 4 CMOS image sensors (LUPA-4000) timing driving, and DDR2 SDRAM data buffering, while it works in series when sending data from each FPGA to ARM and from ARM to PC. Experimental results showed that the data acquisition system worked steadily, and whole images of a custom-built calibration plate were achieved by butting images of the four individual CMOS image sensors' in visible light test environment. This work could be a valuable foundation for realization of all kinds of FOP array coupled digital x-ray detectors.

Keywords: Data acquisition system, fiber optic taper array, multiple CMOS image sensors, x-ray detector.

1. INTRODUCTION

Fiber optic taper (FOT) coupled digital x-ray detector can efficiently reduce the loss of light and achieve high resolution x-ray image. But due to the restriction of FOT large end's size, single fiber optic taper coupled digital x-ray detector can't realize large-area x-ray imaging, which is demanded in medical imaging, macromolecular crystallography, x-ray phase imaging and non-destructive testing [1-5]. FOT array coupled digital x-ray detector formed by FOT array coupled with multiple CCD/CMOS sensors, enlarges the imaging area in multiples, which is an efficient way for large area high resolution digital x-ray imaging [6, 7].

Unique CCD/CMOS based data acquisition system in accordance with the specific geometrical shape of FOT array, has to be designed for FOT array coupled digital x-ray detector, because hardware structures of the data acquisition system are restricted by geometrical shape of the FOT array. Furthermore, data acquisition system should be capable of long distance control in the x-ray radiation environment [8]. Thus it can be seen that besides the ability of properly arranging the sequence of multiple CCD/CMOS sensors' data transmission, data acquisition system must meet lots of conditions, such as fitting to FOT array's geometric shape, long distance control feasibly, high speed and operating Steadily [9]. Data acquisition system is a challenge in development of a digital x-ray detector.

An Ethernet data acquisition system based on FPGA and ARM has been designed and implemented for 2×2 FOT array (with the large end area of 100 mm×100 mm) coupled to 4 CMOS image sensors (LUPA-4000) in this paper. Whole procedures of the data acquisition system have been finished, including hardware and PCB design, timing driving of 4 CMOS image sensors, buffering of image data, Ethernet transmission, storing, butting and display of the images in PC. It is a complex and systematic work involving system structure design, FPGA design, ARM and PC software development.

2. SYSTEM STRUCTURE AND HARDWARE DESIGN

Structure of 2×2 FOT array coupled digital x-ray detector is shown in Fig. (**1**). X-ray scintillator converts incident x-ray into visible fluorescence, and the FOT array guides the fluorescence to photosensitive surfaces of the four CMOS image sensors individually. Output data of every CMOS image sensor are collected by one corresponding Data Acquisition Board, and are buffered in DDR2 SDRAM respectively. Finally data of the four CMOS image sensors' are sent to PC by Data Transmission Board via Ethernet, for image processing, storing and displaying. Introducing of Ethernet interface in this system can overcome the problem of insufficient transmission distance which exists in USB, 1394 or PCI interface system, so it is suitable for long

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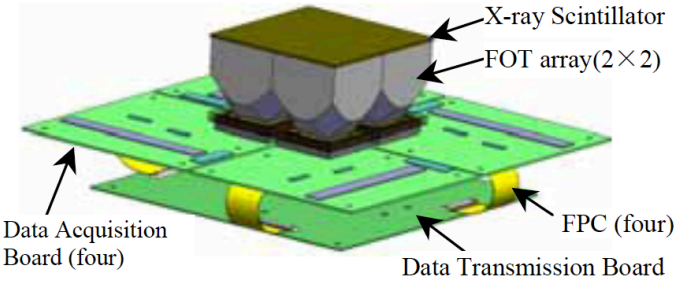


Fig. (1). Structure of 2×2 FOT array coupled x-ray detector.

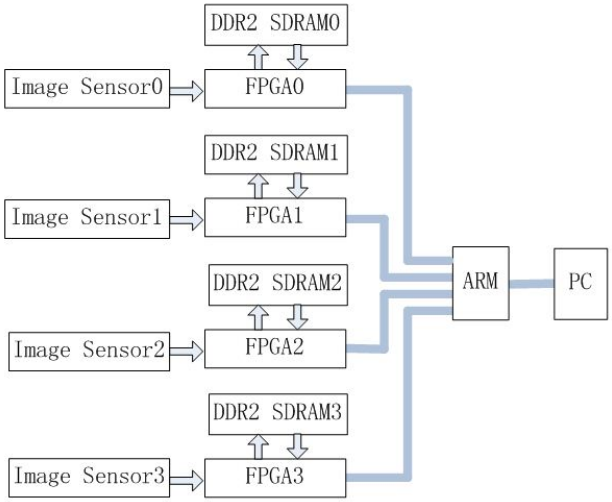


Fig. (2). Principles of the data acquisition system.

distance control in the x-ray radiation environment. Four flexible printed circuit (FPC) were used for connecting Data Transmission Board and the four Data Acquisition Boards, so that relative positions of small ends of FOT array and the four CMOS image sensors can be adjusted, and quality of high speed digital signal transmission can be guaranteed at the mean time.

Principle of the data acquisition system is shown in Fig. (**2**). ARM acts as the main processor, accepts commands from PC and then controls four FPGAs' operations. The four FPGAs perform the operations of data collection, buffering and transmission under the driving of ARM's control signals. LUPA-4000 is an area CMOS image sensor produced by Cypress Inc., with the pixel size of 2048×2048, and the dynamic range can be as large as 90 dB on multiple slope sampling mode.

According to the characters of the data acquisition system, ARM9 chip S3C2410A with ARM920T kernel from Samsung was chosen as the main ARM processor, which is convenient for implementation of Ethernet protocol stack. FPGA chips were Xilinx's I/O ports optimized XC3S400A, which are of abundant I/O ports and are suitable for digital devices' timing driving and logic control. DDR2 SDRAM chips were 1Gbit MT47H64M1625E from Micron, and 25 full frames of LUPA-4000 can be stored in one such a memory chip.

Circuit design of Data Acquisition Board has a critical impact on LUPA-4000's image quality. Seven important power supplies in Data Acquisition Board were designed by adjustable source scheme. For the facts that DDR2 SDRAM would be mounted in Data Acquisition Board, and side length of Data Acquisition Boards' should be as small as possible, causing high density of devices and line routing, Data Acquisition Boards were designed using eight-layers PCB, including four signal layers. Fig. (**3**) shows part of PCB design related to connection lines between FPGA and DDR2 SDRAM. Data Transmission Board was designed using six-layers PCB. Additionally, there are 2.5 mm gaps between adjacent edges of different Data Acquisition Boards, which is necessary for adjusting relative position of each Data Acquisition Board and corresponding small end of FOT array.

3. SOFTWARE AND FPGA DESIGN

Functions of Data Acquisition Board were mainly accomplished by PC, ARM and FPGA. Flow diagram of the data acquisition system is shown in Fig. (**4**). Transmission procedure of control commands and image signals were demonstrated in this figure with emphasis.

Transmission sequence of multiple CMOS image sensors' image data is a difficulty in this system. It can be seen from Fig. (**4**) that parallel and serial procedures were handled alternately in this system. Such procedures as parameters' setting, shooting command's sending, LUPA-4000s' timing driving, and data buffering were handled parallelly, while the procedures of sending image data from individual FPGA to

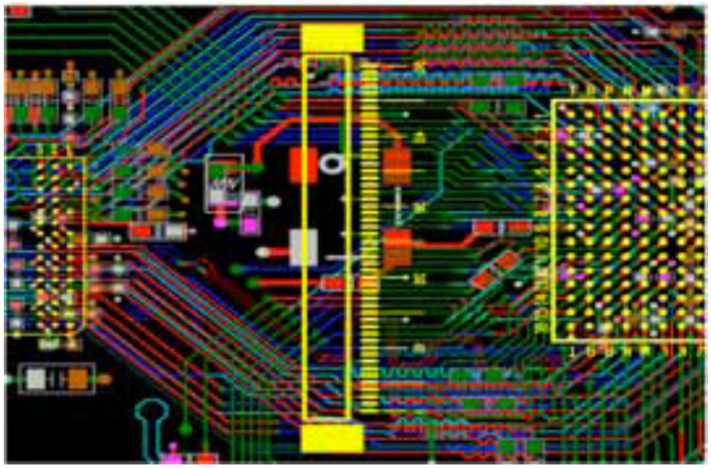


Fig. (3). Part of PCB design related to connection lines between FPGA and DDR2 SDRAM.

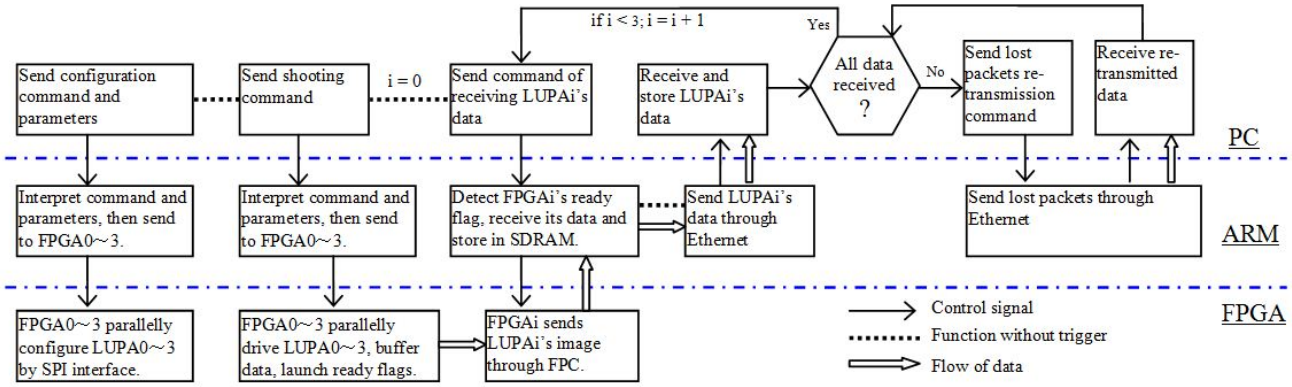


Fig. (4). Flow diagram of the data acquisition system.

ARM, Ethernet transmission, and lost packets retransmission of each CMOS image sensor's image data were handled serially. When data buffering was ready, data transmission procedure as well as lost packets retransmission procedure launched serially from No. 0 CMOS sensor to No. 3 CMOS sensor until all data were sent to PC. This design is easy to be extended, and can be applied for data acquisition systems with larger FOT array, for example 3×3 or 4×4.

(1) Functions Implemented by PC

Functions of PC include sending configuration signals and corresponding parameters to every FPGA, sending shooting command, receiving and storing every CMOS image sensor's image data, image distortion correction and display. PC program of this system was developed by Java language, which is convenient for network programming.

It should be noted that there were geometry and radiometric distortions to a certain extent in achieved images, for seasons such as nonuniformity among different pixels in a single FOT, coupling offsets, and so on. Furthermore, the distortions were not symmetrical in single FOT images, and distortion features were not identical among the four FOTs' images. So it is necessary to correct geometry and radiation distortions of the achieved images in PC.

(2) Functions Implemented by ARM

As the key device of Data Transmission Board, ARM implemented functions including establishing Ethernet protocol stack, receiving configuration and shooting commands from PC and interpreting corresponding parameters, transmitting the commands and parameters to each FPGA, receiving image data from each FPGA and uploading the data to PC.

ARM started to detect FPGA0's FIFO data ready signal after shooting command and corresponding parameters had been sent to FPGAs. Data transmission was performed serially, that is to say ARM would detect the FIFO data ready signal of FPGA0 firstly, and only when the first LUPA-4000's image data had been sent to PC through Ethernet, ARM would start to detect the FIFO data ready signal of FPGA1, and so on. Each FPGA connected to ARM by an internal instantiated asynchronous FIFO, and data ready signal of this FIFO acted as a flag for starting data transmission procedure.

In this implemented data acquisition system, ARM stored each LUPA-4000's image data in the SDRAM of Data Transmission Board before sending them to PC through Ethernet. SDARM storing of image data had the advantage

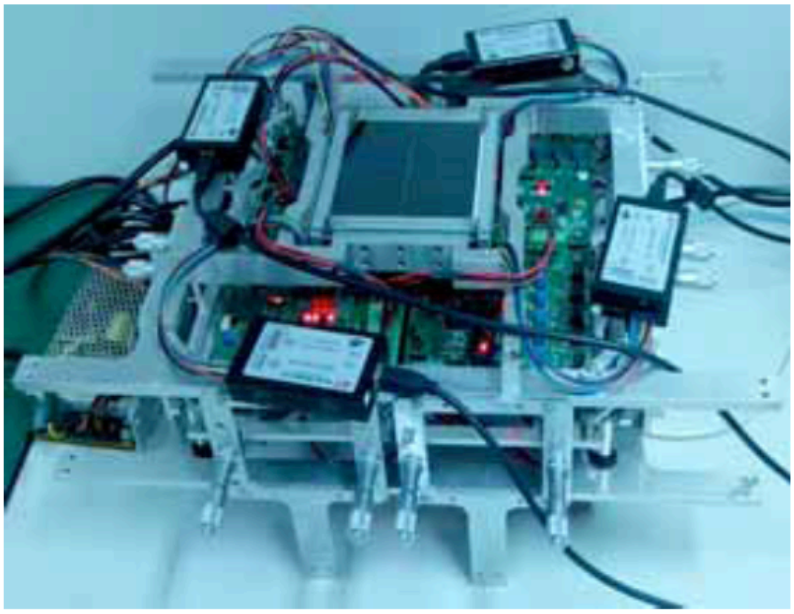


Fig. (5). Photograph of the data acquisition system.

Fig. (6). Screenshot from PC during testing procedure.

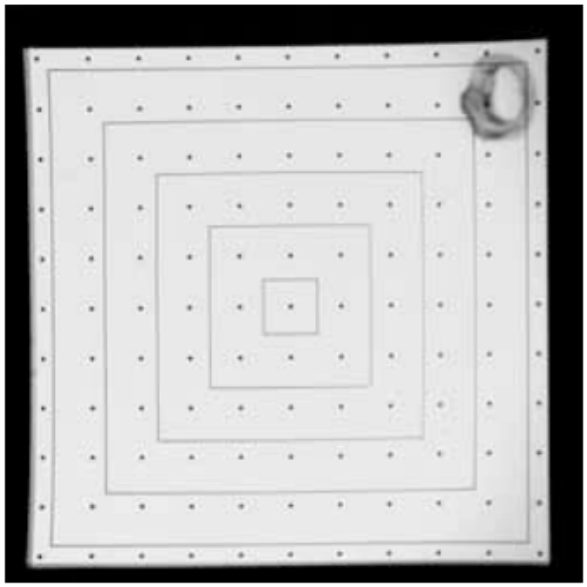
of being convenient for locating the lost packets during data retransmission procedure.

(3) Functions Implemented by FPGA

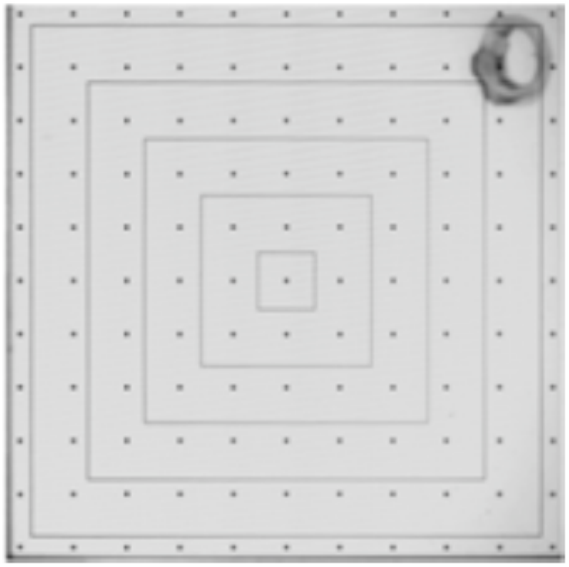
FPGA was the key device of Data Acquisition Board, and was implemented the functions including LUPA-4000's timing driving, DDR2 SDRAM data buffering, interface between LUPA-4000 sensor and DDR2 SDRAM, and interface between FPGA and ARM. These functions involved with some complex FPGA design techniques such as high speed timing driving of CMOS image sensors, DDR2 SDRAM controller, instantiating of asynchronous FIFO, and so on. Detailed description of these functions can refer to relevant references [8, 10].

4. TEST RESULTS OF THE SYSTEM

Photograph of the data acquisition system implemented in this paper is shown in Fig. (**5**). Mechanical structure in



(a) Image of No. 0 LUPA-4000 sensor's before distortion correction



(b) Image of No. 0 LUPA-4000 sensor's with distortion correction

Fig. (7). Tested images of a custom-built calibration plate.

this system was designed for dismountable elastic coupling between the four small ends of FOT array and corresponding LUPA-4000 sensors.

A series of tests had been conducted in visible light environment by varying the parameters such as exposure time, scale of windowing readout, ADC delay time, and so on. Results showed that the data acquisition system worked steadily, and the logic devices, including FPGA and ARM, run normally in repeating experiments. Screenshot from PC during testing procedure is shown in Fig. (**6**). Upper-left section of this figure is the data acquisition system's main control console, which was upgraded from the former single CMOS image sensor's data acquisition system [8]. Lower-left section and Upper-right section show output information of Java development environment and debug information from ARM serial port respectively, and information of these two sections can record the whole process of four LUPA-4000s' data acquisition. Image files stored in PC achieved by the data acquisition system are shown in lower-right section of this figure.

Tested images of a custom-built calibration plate are shown in Fig. (**7**), with the exposure time of 120 microseconds. Fig. (**7a**) is the original image of No. 0 LUPA-4000 sensor's before distortion correction; Fig. (**7**b) is the image of No. 0 LUPA-4000's after 5-order polynomial global correction.

Butted image from the four distortion corrected images of NO.0~3 LUPA-4000 sensors' is shown in Fig. (**8**). It can

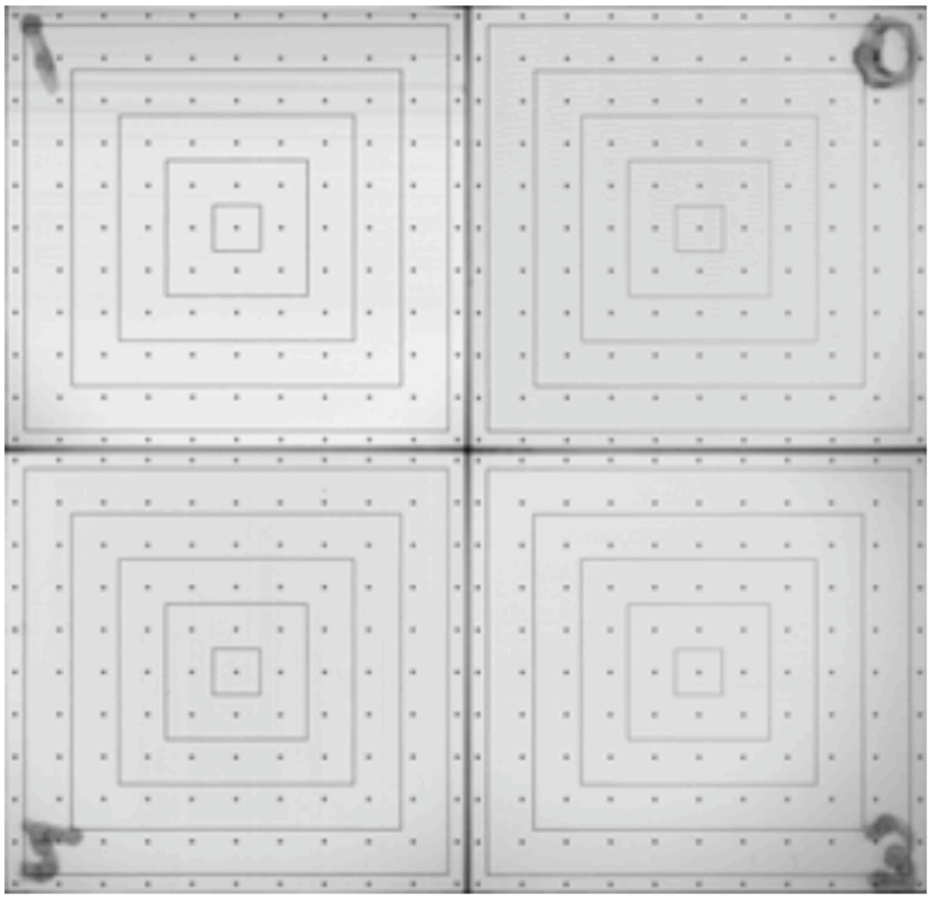


Fig. (8). Butted image from the four distortion corrected images of NO.0~3 LUPA-4000 sensors.

be seen from the images that there are still some geometry and radiation distortions existed in the images. It would be improved in the following research.

CONCLUSION

With the hardware circuit designed in accordance to the shape of 2×2 FOT array, an Ethernet long distance controllable data acquisition system for four CMOS image sensors was implemented in this paper. Resolution of butted images achieved by this data acquisition system is 4096×4096, with the image area as large as 100mm×100mm. During the whole data acquisition process, all the devices including FPGA, ARM and PC, run normally. The multiple CCD/CMOS image sensors data acquisition scheme can be a reference for research and development of high performance FOT array coupled digital x-ray detectors.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

This work was financially supported by China Postdoctoral Science Foundation (Grant No. 2012M511835 and 2013T60813), National Natural Science Foundation of China (Grant No. 61227802), and Specialized Research Fund for the Doctoral Program of Higher Education (Grant No. 20124408120001).

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Received: October 29, 2014 Revised: November 02, 2014 Accepted: November 11, 2014