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Super-Threshold Adiabatic FinFET Circuits Based on PAL-2N Operating in Medium Strong Inversion Regions

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Abstract: Lowering supply voltage of FinFET circuits is an effective way to achieve low power dissipations. In this paper, the super-threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions are addressed in terms of energy consumption and operating frequency. The supply voltage of the super-threshold circuits is much larger than the threshold voltage of the transistors, but it is lower than the normal standard supply voltage. The performance of a mode-10 FinFET PAL-2N counter is investigated with different source voltages ranging from 0.2V to 1.0V. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32nm FinFET technology. The simulation results show that the adiabatic FinFET circuits based on PAL-2N achieve the minimum EDP in the supply voltages of about 700mV - 800mV, the devices of which operate in medium strong inversion regions. The super-threshold adiabatic FinFET logic circuits can attain low energy consumption with favorable performance, since FinFET devices can provide better drive strength than bulk CMOS ones.

Keywords: Adiabatic computing, FinFET circuits, integrated circuits, super-threshold logic, low-power electronics.

1. INTRODUCTION

With the increasing demand for battery-operated electronic systems like laptops, and biomedical applications that require ultra-low energy dissipations, energy-efficient designs of IC (Integrated Circuit) chips have become more and more important [1]. IC designers have been working on high operating speed with low energy dissipations [1-3].

The total energy consumptions in a CMOS circuit mostly include two parts: static energy dissipation caused by leakage currents of MOS devices, dynamic energy dissipations caused by charging and discharging nodes of circuits [4]. The total energy consumption (E_{total}) of a CMOS gate per cycle are expressed as

$$E_{\text{total}} = E_{\text{dyn}} + E_{\text{leakage}} = C_{\text{L}} V_{\text{DD}}{}^{2} + V_{\text{DD}} I_{\text{leakage}} T \quad (1)$$

where C_L is load capacitance of the gate, V_{DD} is source voltage, T is operation cycle, and $I_{leakage}$ is average leakage current from supply to the ground.

In modern CMOS ICs, technology scaling increases the density and performance of a single chip, resulting in large energy consumptions [1, 5]. Meanwhile, the continuing scaling of CMOS devices has greatly increased leakage energy dissipations exponentially, because aggressive scaling reduces the threshold voltage, channel length, and oxide thickness of MOS transistors [5]. Therefore, the continued scaling of MOS device dimension has greatly increased both dynamic and leakage energy dissipations.

From Equation (1), as supply voltage scales down, E_{dyn} is reduced quadratically, and $E_{leakage}$ scales linearly. Therefore, scaling supply voltage is an effective method to reduce the energy consumption of CMOS circuits [6-10]. Sub-threshold computing for CMOS circuits is one of the best solutions to attain low energy consumptions [6, 7]. However, the performance of the sub-threshold CMOS circuits is much lower than these circuits operating on standard source voltages. This is because that the delay of CMOS circuits increases exponentially as the supply voltage scales down. Therefore, sub-threshold computing for CMOS circuits only fits some ultra-low-speed applications [6, 7].

In recent years, near-threshold computing for CMOS circuits is proposed [8, 9]. The supply voltage of near-threshold CMOS circuits is slightly above the threshold voltage of the MOS transistors [9]. The near-threshold CMOS circuits can retain much of the energy savings of sub-threshold circuits [9, 10]. Compared with sub-threshold circuits, the near-threshold CMOS circuits can obtain good performance due to large turn-on currents. However, the near-threshold CMOS circuits are only suitable for mid-speed applications, since their MOS devices operate on medium weak inversion.

With the continuing scaling of CMOS processes, leakage energy dissipations are becoming the main source of energy consumptions [5]. In order to cope with this problem, several novel devices have been developed. FinFET (Fin-type Feld-Effect Transistors) devices show excellent performance with low-power characteristic in the novel devices [11]. The recently reported researches have shown that FinFET is a promising alternative for the CMOS processes to realize continued scaling, since it can well suppress the short-channel effects and gate-dielectric leakage current [11-13].

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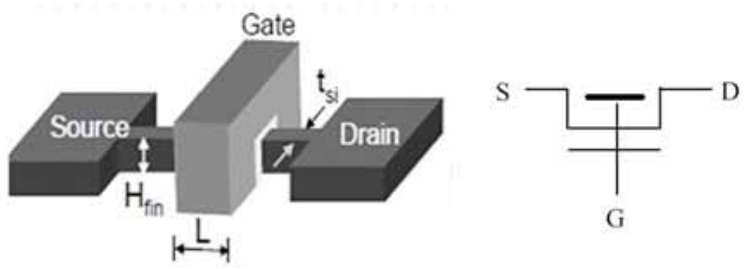

Fig. (1). Structure and symbol of FinFET.

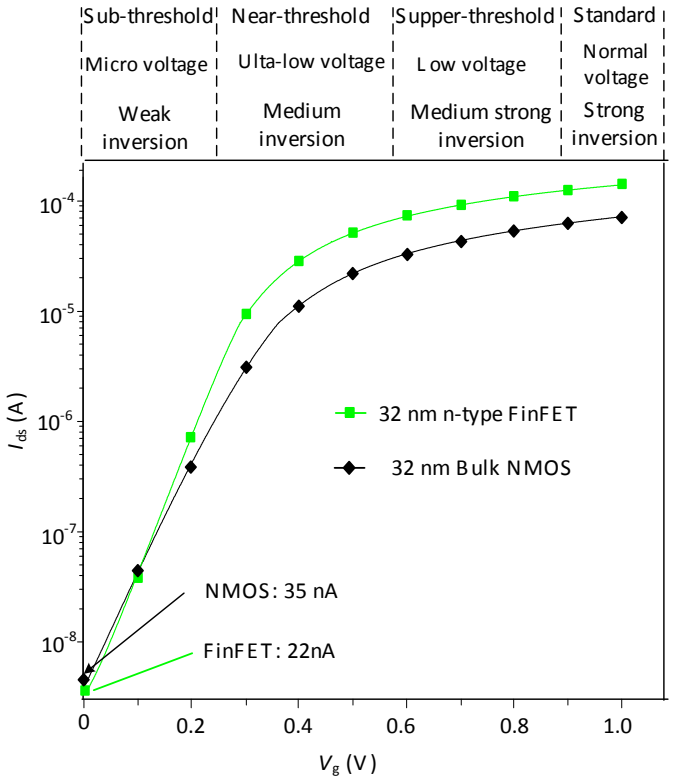

Fig. (2). I -V characteristics of 32 nm n-type FinFET and NMOS bulk transistors.

In this paper, super-threshold adiabatic FinFET circuits based on PAL-2N (Pass-transistor adiabatic logic with NMOS pull-down configuration) are presented in terms of energy consumption and operating frequency. All circuits are simulated with HSPICE at a 32nm PTM (Predictive Technology Model) FinFET technology [14]. The supply voltage of the super-threshold circuits is much larger than threshold voltage of the transistors, but it is lower than standard supply voltage. In super-threshold circuits, the devices operate in medium strong inversion regions, and thus more favorable performance can be obtained compared with near-threshold circuits. Meanwhile, super-threshold FinFET circuits retain most energy savings of near-threshold operation. Since FinFETs can provide stronger drive strength than the conventional CMOS, the super-threshold adiabatic FinFET logic circuits can attain favorable performance with low energy consumption.

2. ENERGY DISSIPATION AND DELAY OF FINFET CIRCUITS

The FinFET is a three-dimensional device, as shown in Fig. (**1**), which consists of a thin silicon body, the thickness of which is denoted by t_{Si} . In FinFETs, gate electrodes wrap the thin silicon body. The FinFET channel is formed perpendicular to the plane of the wafer. The currents flow parallel to the wafer plane. FinFETs are double-gate devices, and the two gates can either be shorted or independently controlled. The independent front and back gates can be achieved by etching away the gate electrode at the top of the FinFET device [12, 13]. In this work, only short-gate (SG) mode is considered. The effective gate width of a SG FinFET transistor is $2nH_{fin}$, where n is fin number and H_{fin} is fin height. The wider transistors can be obtained by using multiple fins.

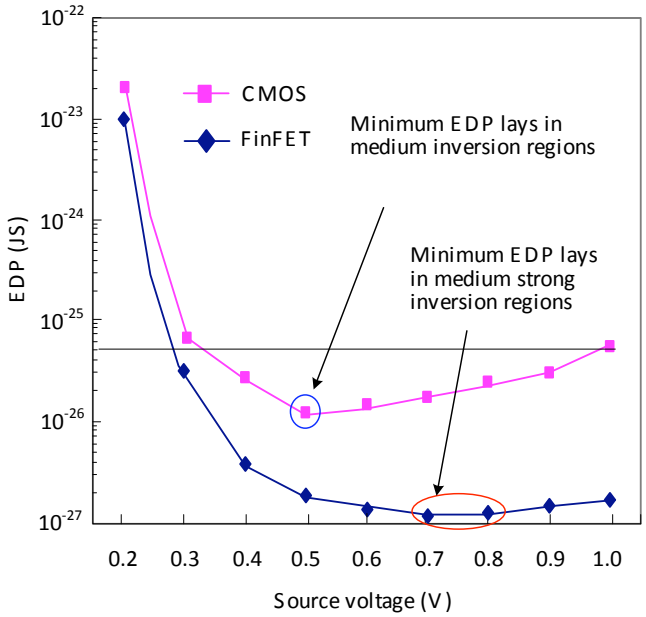

Fig. (3). EDP comparisons of 32nm FinFET and conventional bulk CMOS inverters.

The simulation results for the I-V characteristics of 32 nm n-type FinFET and conventional bulk NMOS are shown in Fig. (**2**). Compared with conventional bulk NMOS, the FinFET transistor has high turn-on current, and thus fast operating speed. Therefore, FinFET logic circuits operating on medium inversion regions and strong inversion regions can obtain more favorable performance than conventional bulk CMOS. In addition, super-threshold FinFET logic circuits operating on medium strong inversion regions can obtain faster speed than near-threshold ones operating on medium inversion regions.

As shown in Fig. (**2**), the FinFET device has larger sub-threshold slope than conventional MOS transistors due to strong gate control over the channel. Compared with bulk MOS transistors, the leakage of the FinFET ones is reduced significantly.

Assuming that symmetrical P-type and N-type transistors are used, the delay of an inverter in medium inversion and strong inversion regions can be expressed as

$$t_d = \frac{KC_L V_{DD}}{\left(V_{DD} - V_{th}\right)^{\alpha}} \tag{2}$$

where K is a delay fitting parameter, a is velocity saturation parameter, and V_{th} is threshold voltage.

In sub-threshold regions, the delay of an inverter can be expressed as

$$t_d = \frac{KC_L V_{DD}}{I_{o,g} \exp\left(\frac{V_{DD} - V_{th,g}}{nV_T}\right)} \tag{3}$$

where V_T is the thermal voltage, n is the sub-threshold slope factor, and $I_{0,g}$ and $V_{th,g}$ are fitting parameter, respectively.

EDP (Energy Delay Product) metric provides a good compromise between energy consumption and operating speed, which is

$$EDP = E \times t_{delay} \tag{4}$$

The EDP of an inverter is given by plugging Equation (1), Equation (2), and Equation (3) into Equation (4)

$$EDP = \begin{cases} \dfrac{\left(C_L V_{DD}^{\ 2} + V_{DD} I_{leakage} T\right) KC_L V_{DD}}{\left(V_{DD} - V_{th}\right)^{\alpha}} & V_{dd} > V_{th} \\ \dfrac{\left(C_L V_{DD}^{\ 2} + V_{DD} I_{leakage} T\right) KC_L V_{DD}}{I_{o,g} \exp\left(\dfrac{V_{DD} - V_{th,g}}{nV_T}\right)} & V_{dd} < V_{th} \end{cases} \tag{5}$$

The energy delay product of the inverters based on 32nm FinFET and conventional bulk CMOS is shown in Fig. (**3**). For conventional bulk CMOS inverters, PMOS transistors are taken with W/L = 96 nm / 30 nm, NMOS transistors are taken with W/L = 45 nm / 30 nm. For FinFET inverters, the fin number n is P-type and N-type transistors is 2 and 1, respectively.

The FinFET inverter performs smaller PDP than CMOS in all source voltages. The FinFET inveter achieves the minimum EDP at the supply voltage of about 700mV - 800mV, which is lays in medium strong inversion regions, while the EDP of the CMOS inverter is minimized at about 500mV, which is lays in medium inversion regions. Therefore, near-threshold computing for CMOS circuits can obtain optimal EDP, while super-threshold FinFET circuits can achieve minimum EDP. As shown in Fig. (**3**), the FinFET inverter provide a reduction of about 90% compared with the CMOS one in term of the minimum EDP.

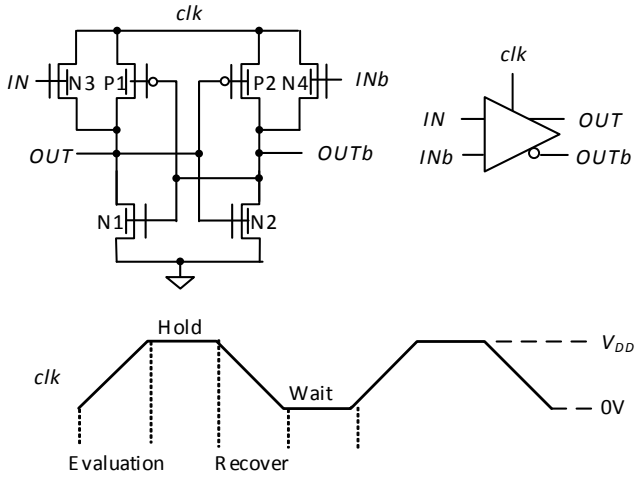

Fig. (4). FinFET buffer/inverter based on PAL-2N: schematic, symbol, and power clock.

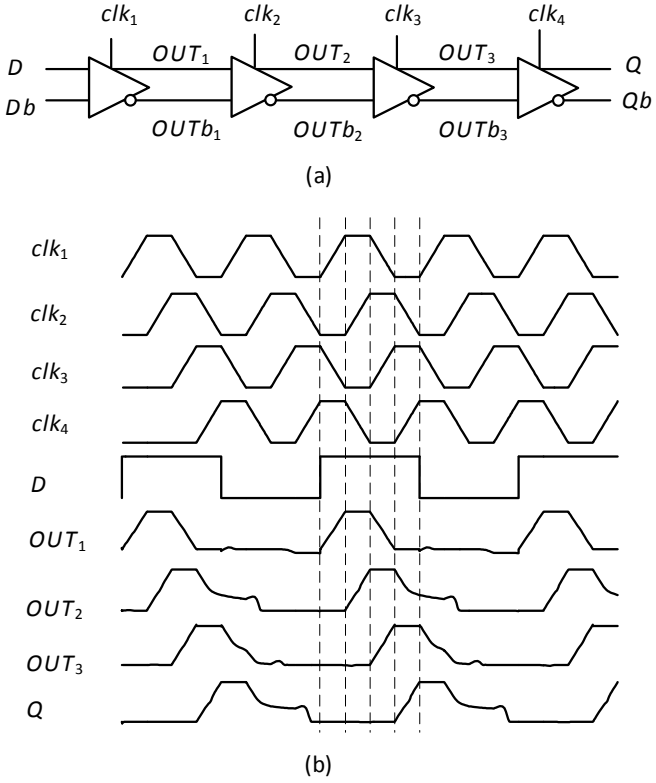

Fig. (5). FinFET PAL-2N flip-flop. (a) *D* flip-flop, and (b) Simulation waveforms of *D* flip-flop.

3. ADIABATIC FINFET LOGIC CIRCUITS BASED ON PAL-2N

The FinFET PAL-2N buffer/inverter is shown in Fig. (**4**) [15]. It is composed of three main parts: the evaluation circuit consists of N-type FinFET transistors trees (N3 and N4) implementing logic function. The load driven circuit consists of a pair of P-type FinFET transistors (P1 and P2) for recovering energy into power clock. The clamp FinFET transistors (N1 and N2) providing a well-defined output logic '0'. The power-clock supply *clk* is a trapezoidal or sinusoidal waveform. It has the four phases: evaluation when the power clock *clk* is ramping up, hold when *clk* is keeping stable high, recovery when *clk* is ramping down, and wait when the power clock *clk* is keeping stable low for symmetry waveforms.

Assuming that *IN* and *INb* are low and high, respectively, the N-type FinFET transistor N4 is turned on. During the evaluation phase, when the power clock *clk* ramps up, *OUTb* follows *clk*. When *OUTb* exceeds V_{TN} (threshold voltage of the N-type FinFET transistors), N1 is turned on, providing a conducting path from *OUT* to ground. The p-type transistor P2 is then switched on, and thus *OUTb* follows *clk* unto V_{DD}. During the recovery phase, the power clock *clk* ramps down, *OUTb* follows *clk* down through P2 and N4. When *clk* drops below $|V_{TP}|$ (threshold voltage of P-type transistors), P2 is turned off and *OUTb* follows *clk* through N4 to 0V.

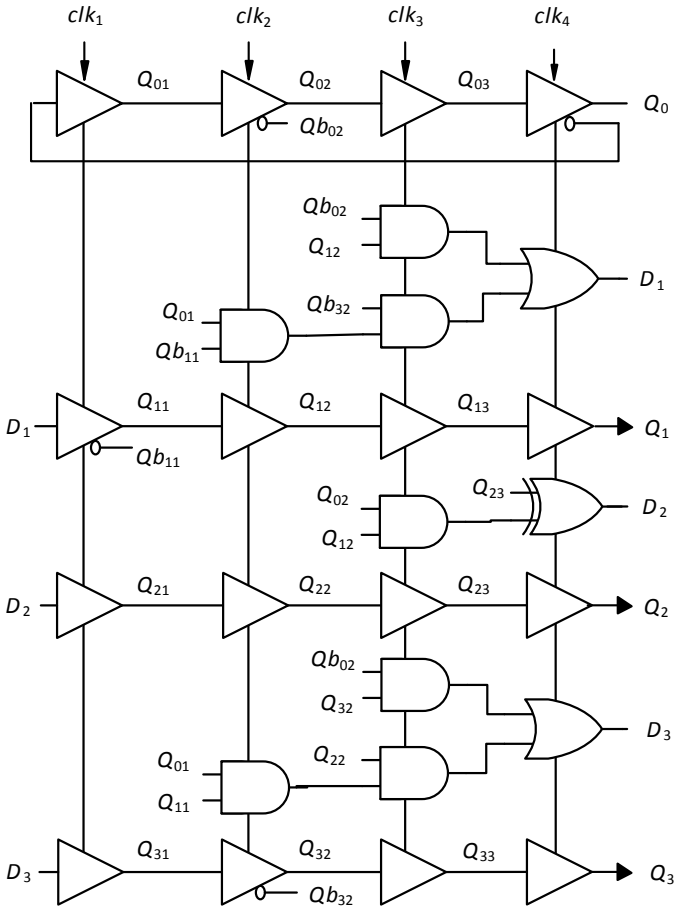

Fig. (6). Adiabatic FinFET mode-10 counter based on PAL-2N circuits.

Complex logic circuits can be derived simply by replacing the N-type pass transistors trees with the corresponding logic blocks. *D* flip-flop is illustrated in Fig. (**5a**). The four trapezoidal clocks (clk_1 - clk_4) with 90 phase lag are used. Its simulated waveforms is shown in Fig. (**5b**).

A mode-10 adiabatic counter based on FinFET is shown in Fig. (**6**), which consists of four *D* flip-flops. The Boolean expressions of Q_0–Q_3 are written by

$$\begin{aligned} D_0 &= Q_0^{n+1} = \overline{Q_0^n} \\ D_1 &= Q_1^{n+1} = \overline{Q_3^n}\,\overline{Q_1^n} Q_0^n + Q_1^n \overline{Q_0^n} \\ D_2 &= Q_2^{n+1} = Q_2^n \oplus Q_1^n Q_0^n \\ D_3 &= Q_3^{n+1} = Q_2^n Q_1^n Q_0^n + Q_3^n \overline{Q_0^n} \end{aligned} \tag{6}$$

4. SIMULATIONS OF SUPER-THRESHOLD ADIABATIC FINFET CIRCUITS

In order to investigate the performances of the PAN-2N circuits based on FinFET in sub-threshold, near-threshold, and super-threshold regions, the PAL-2N FinFET mode-10 counters are simulated with different peak-to-peak voltages of the power clocks ranging from 0.2V to 1.0V with 0.1V step using the 32nm FinFET PTM technology. For the PAL-2N gates of the mode-10 counter, the fin number *n* of all P-type FinFET is taken with 2. The fin number of the clamp N-type FinFET is taken with 1, and the fin number of all the evaluation N-type FinFETs is taken with 2.

4.1. Energy Consumptions of the FinFET PAL-2N Counter at 1 MHz

Fig. (**7**) shows the energy consumption of the FinFET mode-10 counter based on PAL-2N with various peak-to-peak voltages (V_{DD}) of the power clocks at 1 MHz. Scaling down the supply voltage can save energy consumptions effectively. The energy consumption of the counter at 0.2V and 0.8V supply voltage is only 1.66% and 48.2% of that of 1.0V supply voltage, respectively.

4.2. Max Operating Frequency and Energy Consumptions of the FinFET PAL-2N Counter

In order to obtain the maximum operating frequency of the FinFET counter in various peak-to-peak voltages of the power clocks, HSPICE simulations have been carried out with various peak-to-peak voltages and frequencies. Maximum operation frequency of the FinFET mode-10 counter based on PAL-2N is obtained, where the counter has correct logic function, as shown in Fig. (**8**). As the peak-to-peak voltages of the power clocks scales down, the maximum operating frequency and energy dissipation is reduced.

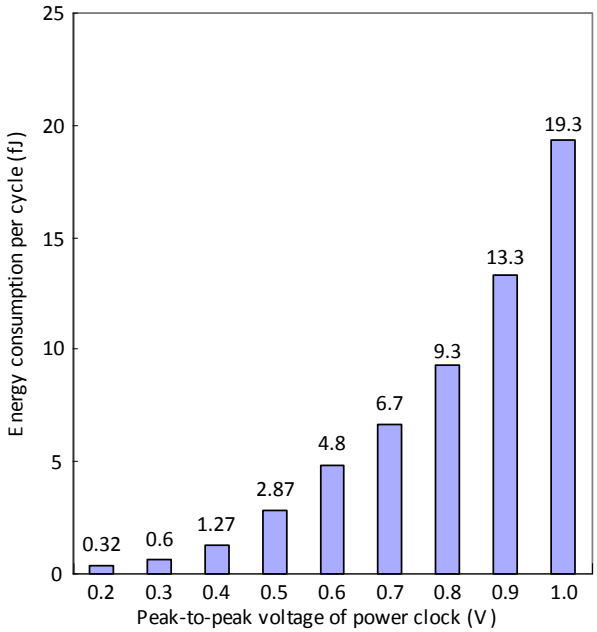

Fig. (7). Energy consumptions of the FinFET mode-10 counter based on PAL-2N from 0.2V to 1.0V at 1 MHz.

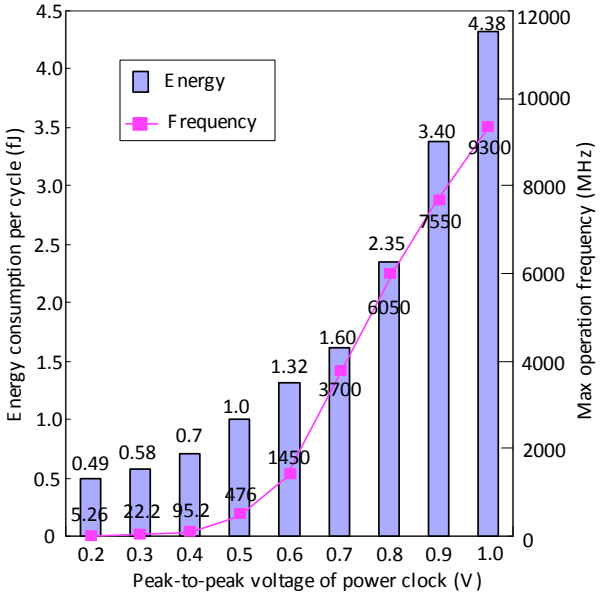

Fig. (8). Max operating frequency and corresponding energy consumptions of the FinFET mode-10 counter based on PAL-2N from 0.2V to 1.0V supply voltages.

The maximum operating frequency of the FinFET counter based on PAL-2N at 0.2V is only 0.057% of that of 1.0V peak-to-peak voltage. Although the minimum energy consumption is reached at sub-threshold regions, it only fits for ultra-low speed application, where the energy dissipation of the FinFET counter is only 11.2% of that of 1.0V peak-to-peak voltage.

At 0.5V and 0.6V peak-to-peak voltage of the power clock, the energy dissipation of the adiabatic FinFET mode-10 counter is only 22.8% and 30.0% of that of 1.0V peak-to-peak supply voltage, respectively. However, the maximum operating frequency of the adiabatic FinFET counter at 0.5V and 0. 6V is only 5.1% and 15.6% of that of 1.0V peak-to-peak supply voltage. Therefore, near-threshold adiabatic circuits based on FinFET operating in medium inversion regions fit for mid-performance applications with low energy consumption.

At 0.8V peak-to-peak voltage of the power clock, the energy dissipation of the adiabatic FinFET counter is only 53.6% of that of 1.0V supply voltage. The maximum operating frequency of the adiabatic FinFET counter at 0.8V is 65.1% of that of 1.0V supply voltage. Therefore, super-

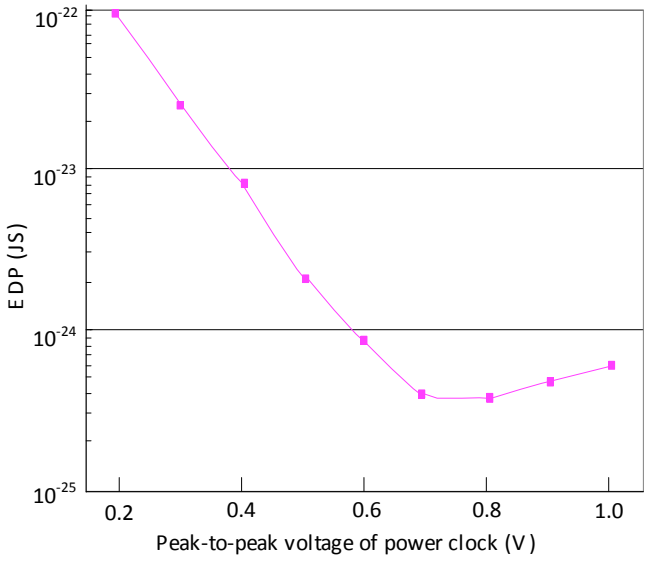

Fig. (9). EDP of the FinFET mode-10 counter based on PAL-2N from 0.2V to 1.0V supply voltages.

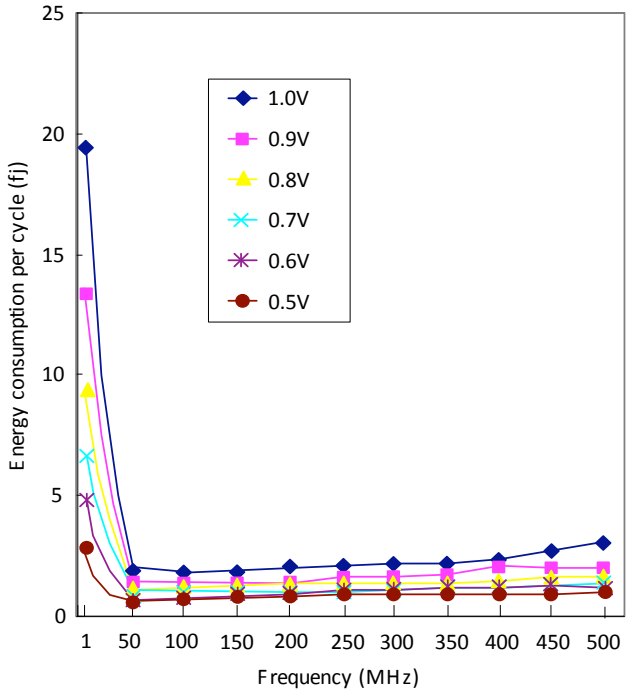

Fig. (10). Energy consumptions per cycle of the FinFET mode-10 counter based on PAL-2N from 1MHz to 500MHz with various source voltages.

threshold adiabatic FinFET circuits operating on medium strong inversion regions attain considerable energy reduction with an acceptable penalty in operating speed compared with near-threshold ones.

EDP of the FinFET mode-10 counter based on PAL-2N for deferent peak-to-peak voltage of the power clock is shown in Fig. (**9**). EDP of adiabatic circuits is defined as

$$EDP = \frac{E_{adiabatic}}{f_{\max}} \quad (7)$$

where, $E_{adiabatic}$ is energy consumption per cycle, and f_{max} is maximumoperating frequency. The PAL-2N FinFET mode-10 counter achieves the minimum EDP at the supply voltage of about 700mV -800mV, where the device of the circuits operates in medium strong inversion regions. The FinFET mode-10 counter based on PAL-2N operating in optimum supply voltages provide an EDP reduction of 17.5% as compared to nominal supply voltage operation (1.0V).

4.3. Performance of the FinFET Counter Based on PAL-2N at Various Supply Voltages

Fig. (**10**) shows the energy consumption of the FinFET mode-10 counter from 1MHz to 500MHz with various source voltages. In low operating frequencies, as the fre-

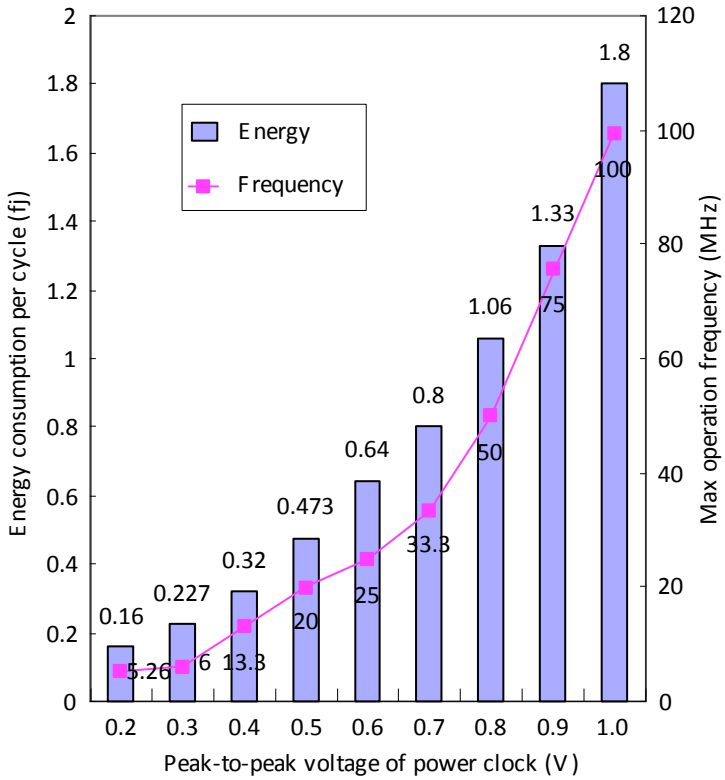

Fig. (11). Minimum energy consumption per cycle and corresponding operating frequency of the mode-10 counter based on FinFET from 0.2V to 1.0V.

quency is reduced, the energy consumption increases dramatically. In high operating frequencies that are larger than about 50MHz, the energy consumption rises slightly as the frequency increases since the dynamic energy dissipations of the adiabatic circuits increase as operating frequencies. At 0.7V peak-to-peak voltage of the power clock, the energy consumption of the counter operating in 250MHz and 500MHz can save 50% and 56.6% compared with the nominal supply voltage, respectively.

As is mentioned above, the leakage energy consumption of the adiabatic circuits is increases as the frequency is reduced, while the dynamic energy consumption of the adiabatic circuits rises as the frequency increases. Therefore, for a constant supply voltage, the minimum energy consumption per cycle of the FinFET mode-10 counter based on PAL-2N can be reached by varying operating frequency, as shown in Fig. (**11**). In Fig. (**11**), the corresponding operating frequency is also shown when the FinFET mode-10 counter based on PAL-2N obtains minimum energy consumption.

Compared with nominal supply voltage operation, the minimum energy consumption of the FinFET mode-10 counter based on PAL-2N saves 41.1% at 0.8V peak-to-peak voltage of the power clock. At 0.8V and 1.0 peak-to-peak voltage of the power clock, when the FinFET mode-10 counter based on PAL-2N obtains minimum energy consumption, the corresponding operating frequency is about 50MHz and 100MHz, respectively.

4.4. Energy Consumption Comparison Between FinFET and Conventional FinFET Circuits

The energy consumption of the adiabatic FinFET counter has been compared with the conventional FinFET counter at 0.8V source voltage, as shown in Fig. (**12**). The conventional FinFET mode-10 counter is realized by using the transmission gate master-slave (TGMS) flip-flop.

The super-threshold FinFET counter based on PAL-2N shows significant improvement in terms of energy consumption. The energy consumption saving of the FinFET counter based on PAL-2N is 86.7%, 76.67% and 72.7% at 1MHz, 250MHz and 500MHz operating frequency, respectively compared with the conventional FinFET counter using the DC supply source.

CONCLUSION

Lowering supply voltage of FinFET circuits is an effective way to achieve low power dissipations. The super-threshold adiabatic FinFET circuits based on PAL-2N operating on medium strong inversion regions have been addressed in terms of energy consumption and operating frequencies. The performance of a mode-10 FinFET PAL-2N counter has also been investigated with different source voltages ranging from 0.2V to 1.0V.

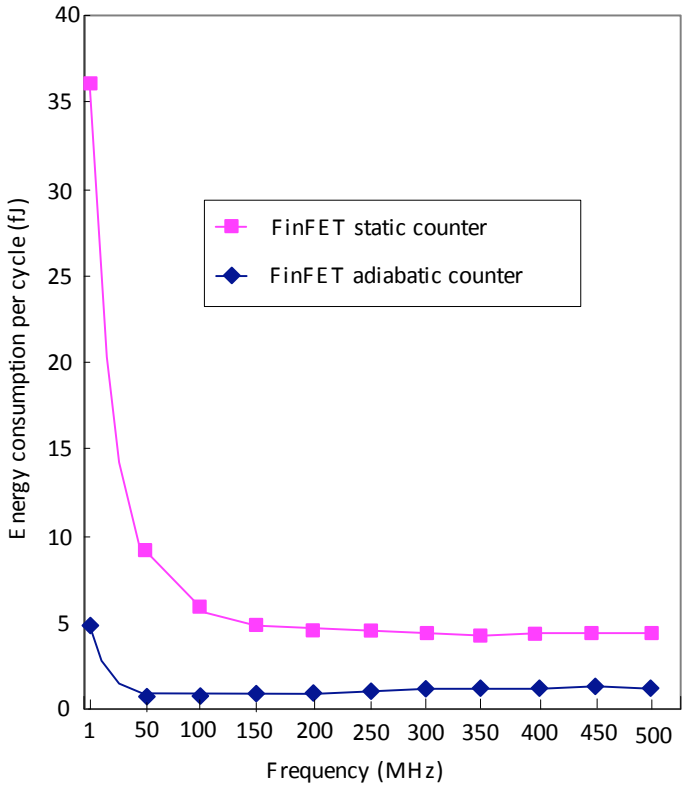

Fig. (12). Energy dissipation comparisons between FinFET adiabatic and conventional mode-10 counters at 0.8V supply voltage.

The simulation results show that the PAL-2N FinFET mode-10 counter achieves the minimum EDP at the supply voltage of about 700mV -800mV, where the device of the circuits operates in medium strong inversion regions. The FinFET PAL-2N mode-10 counter operating in optimum supply voltages provide an EDP reduction of 17.5% as compared to nominal supply voltage operation (1.0V). At 0.8V peak-to-peak voltage of the power clock, the energy dissipation of the adiabatic FinFET counter is only 53.6% of that of 1.0V supply voltage, and the maximum operating frequency is 65.1% of that of 1.0V supply voltage. Therefore, The super-threshold adiabatic FinFET logic circuits can attain low energy consumption with favorable performance, since FinFET devices can provide better drive strength than bulk CMOS ones.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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