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A Power-Gating Scheme for MCML Circuits with Separable-Sizing Sleep Transistors

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Abstract: Power-efficient designs are essential for micro-power sensor systems. This paper presents a power-gating scheme for MCML (MOS Current Mode Logic) circuits with separable-sizing sleep transistors. In the proposed scheme, two high-threshold power-gating transistors are inserted between load transistors and outputs of the MCML circuits. The widths and lengths of sleep transistors in power-gated blocks are separately adjusted, which are independent of the bias circuit. Basic cells and a 1-bit full adder are used to verify the correctness of the proposed scheme. The power consuming comparisons between conventional MCML and proposed power-gating MCML circuits are carried out. The 1-bit MCML full adder based on the proposed scheme nearly saves 36% of energy dissipations with respect to no-power-gating MCML one, for a power-gating activity of 0.6. Moreover, the proposed power-gating MCML circuit also has a great advantage in power dissipations in high frequency regions compared with the power-gating static CMOS ones. The power consumption of the MCML 1-bit full adder based on the proposed scheme is 63.2%, 44.8%, and 36.97% compared with the power-gating static CMOS one when the operating frequency is 1GHz, 1.5GHz, and 2GHz, respectively.

Keywords: Energy efficient design, low power electronics, micro-power systems, MOS current mode logic, power-gating scheme.

1. INTRODUCTION

Nowadays, energy is one of the most important factors in circuit designs. Besides, the importance of energy-efficient becomes greater than before, as the number of micro-power sensor systems and portable computers grow drastically [1]. The origin of power dissipation in traditional CMOS circuits can be divided into dynamic and static dissipations, and thus the expression of total power dissipation can be listed as

$$E_{total} = E_{dyn} + E_{leakage} = C_L V_{DD}^2 + V_{DD} I_{leakage} T \quad (1)$$

Where, E_{dyn} is the dynamic dissipation, $E_{leakege}$ is the static consuming, C_L represents the load capacitance, V_{DD} means the source voltage, $I_{leakage}$ is the leakage current, and T is the operation cycle, respectively.

Traditionally, the dynamic power consuming dominates the total power dissipation, while the leakage power dissipation is so little and thus often neglected [2]. However, with the CMOS technology scaling into deep sub-micro processes, leakage consuming catches up with the dynamic power dissipation. The leakage consumption has become one of the most important factors in low-power hardware [3]. From (1), $E_{leakage}$ decreases linearly with the reduction of source voltage V_{DD}. Besides, in a complex circuit, not every block operates all the time. If the source voltage is cut down when the block works in sleep mode, energy can be saved efficiently. Therefore, power gating techniques have widely been addressed to reduce standby power dissipations [3, 4].

In MOS Current Mode Logic (MCML) circuits, logic *1* is expressed by the source voltage V_{DD}, while logic *0* can be represented as V_{DD} - ΔV (ΔV means the output voltage swing). It is easy to know that the swing of MCML circuits is much little than conventional CMOS circuits [5, 6]. That is a main reason why the circuits designed by MCML can operate over a much higher speed than traditional CMOS [5].

The power dissipation of MCML circuits is not related to operating frequencies, and thus the power consumption of MCML circuits is lower than the conventional CMOS ones in high speed applications [7, 8]. However, this feature also leads to a disadvantage that the power consuming of MCML circuits is much larger than the static CMOS ones for low-frequency operating [9].

As mentioned above, power gating is an effective way to reduce the steady leakage power consuming of static CMOS circuits. Similar to the static CMOS, MCML circuit can also be power-gated to reduce the power dissipations in sleep mode. A fine-grain power gating method is proposed by Alessandro Cevrero *et al.*, in which every basic cell contains a sleep transistor [10]. The results shows that static power consumption is significantly reduced with a delay penalty of 2.7% and area overhead of about 5.6% for basic logic cells such as AND/NAND and multiplexer gates. A reduced swing logic style that named as dynamic current mode logic has been put forward [11]. However, it has a bad noise margin with complex structure.

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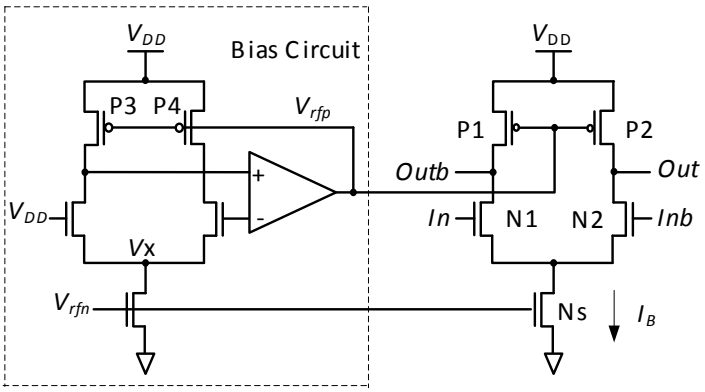

Fig. (1). MCML inverter/buffer and its bias circuit.

In this work, two high-threshold power-gating transistors are inserted between load transistors and outputs as power-gating switches. The widths and lengths of sleep transistors in power-gated blocks are separately adjusted, which are independent of the bias circuit. Therefore, all the proposed power-gating MCML circuits only need one bias circuit. The equivalent model for calculating energy dissipations of the power-gating MCML circuits is constructed. The optimization methods for sizing power-gating transistors are also addressed in term of power dissipations.

2. MCML CIRCUITS

Fig. (**1**) shows MCML buffer/inverter (right) and its biasing circuits (left). The MCML buffer/inverter consists of three parts. The first part is the load transistors P1 and P2. The second part is the full differential pull down switch network N1 and N2. The third part is the current source transistor Ns. The load transistors operate in linear region under the control of voltage V_{rfp} that is produced by the bias circuit. Besides, the signal V_{rfp} controls the logic swings of outputs. NMOS transistors N1 and N2 constitute the pull-down network (PDN), which performs logic operation. The constant current source I_B is supplied by the NMOS transistor Ns. This current source is mirrored from the bias circuit. This structure of MCML circuits determines that the output of logic 1 and logic 0 is $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD}–I_B \times R_D$, respectively. R_D represents the equivalent load resistance of the PMOS transistors. The output swing is $\Delta V = V_{OH} – V_{OL} = I_B \times R_D$.

Realization methods of the PDN of MCML are similar to differential logic styles such as DCVSL and DSL. All basic cells can be realized by replacing the NMOS N1 and N2 with differential logic trees.

Easily, the formulas of MCML power consumption and energy consumption can be expressed as

$$P = NV_{DD}I \tag{2}$$

$$E = PT = NV_{DD}IT, \tag{3}$$

Where, N represents the cascade number of gates, V_{DD} means the source voltage, I is the source current, and T means the operation time.

From (3), to reduce the energy consumption, an immediate solution is scaling down the supply voltage, because the total energy can reduce linearly with the decreasing of supply voltage. However, normal source voltage must be provided to ensure the performance of circuits when the cells are operating. In other words, to avoid the needless energy waste, the supply voltage of blocks can be cut off when the blocks are not working.

3. POWER-GATING SCHEME

Power gating can reduce the standby energy dissipation of circuits by inserting power-gating switches to the supply voltage path. There are kinds of ways to achieve power-gating MCML circuits. A typical power-gating structure is shown in Fig. (**2**) [12].

In Fig. (**2**), the load PMOS transistors in MCML circuits are set as high-threshold devices to reduce the sleep power dissipation. An advantage of this realization scheme is that it has no additional propagation delay and area overhead. However, as is shown in Fig. (**2**), the widths and lengths of load PMOS transistors must be the same in all the power-gated modules if only a bias circuit is used. Otherwise, more than one bias circuit is needed to ensure the proper performance of the power-gating MCML circuits. Once the widths of P1 and P2 are changed, the widths and lengths of PX and PY in bias circuit should be adjusted. Therefore, when the widths and lengths of the load PMOS transistors are different, there are many bias circuits in the MCML circuits that adopt this power-gating scheme. The area and power dissipation can increase inevitably with these extra bias circuits.

In this paper, a new scheme is presented, where the widths and lengths of sleep transistors in power-gated blocks are independent of the bias circuit, as shown in Fig. (**3**). In the proposed scheme, the widths and lengths of sleep transistors in various circuits can be different. Therefore, less bias circuits are needed in the complex circuit compared to the conventional power-gating MCML one.

The power-gating MCML basic gates that based on the proposed scheme such as AND2/NAND2 and XOR2/XNOR2 are shown in Fig. (**4**). In Fig. (**4**), if the control signal *Sleep* is 0, P3 and P4 are turning on, and thus the circuit operates in active mode. On the contrary, when the

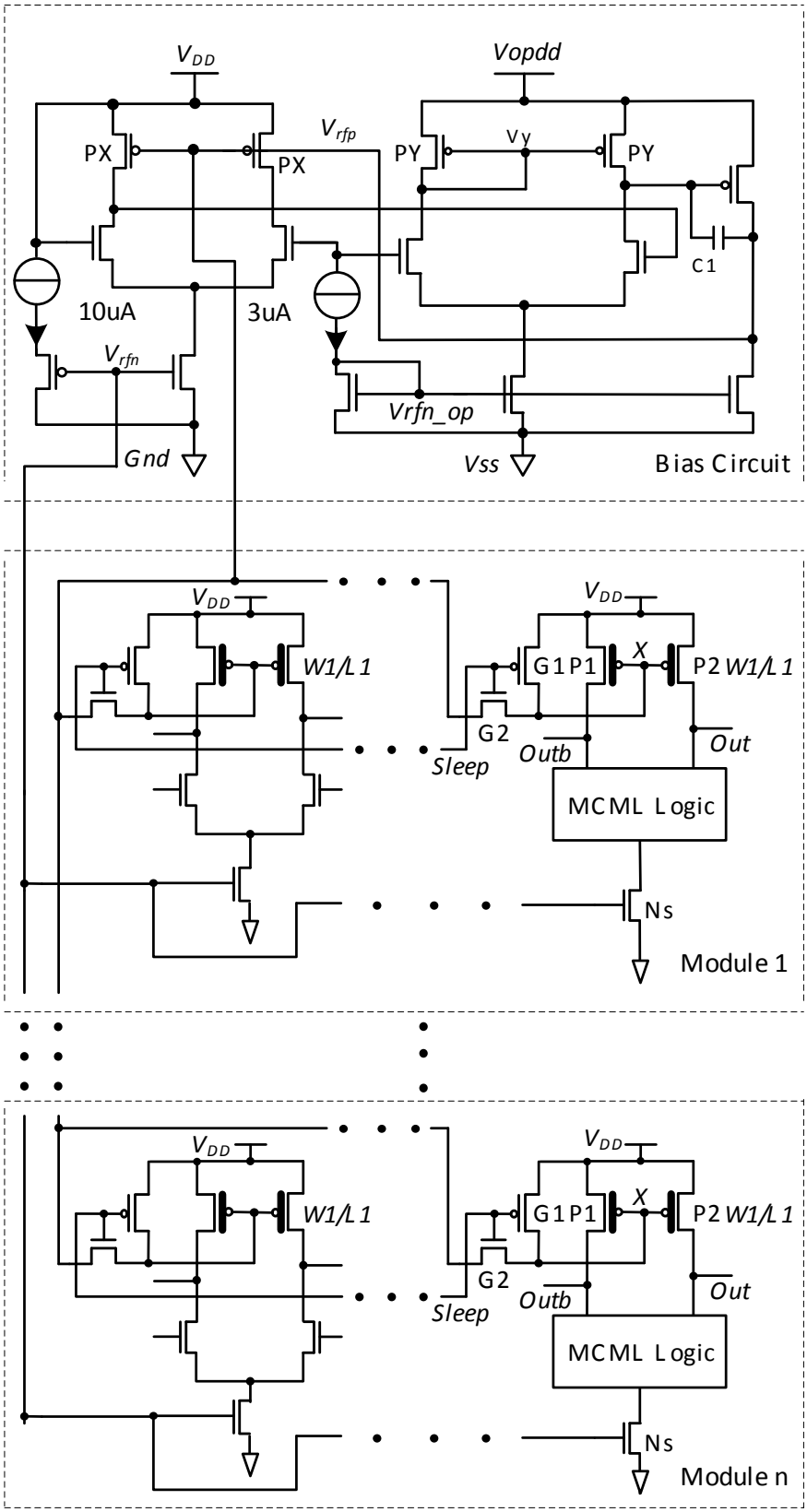

Fig. (2). Power-gating MCML circuits whwer the widths and lengths of sleep transistors in power-gated blocks are dependent on the bias circuit.

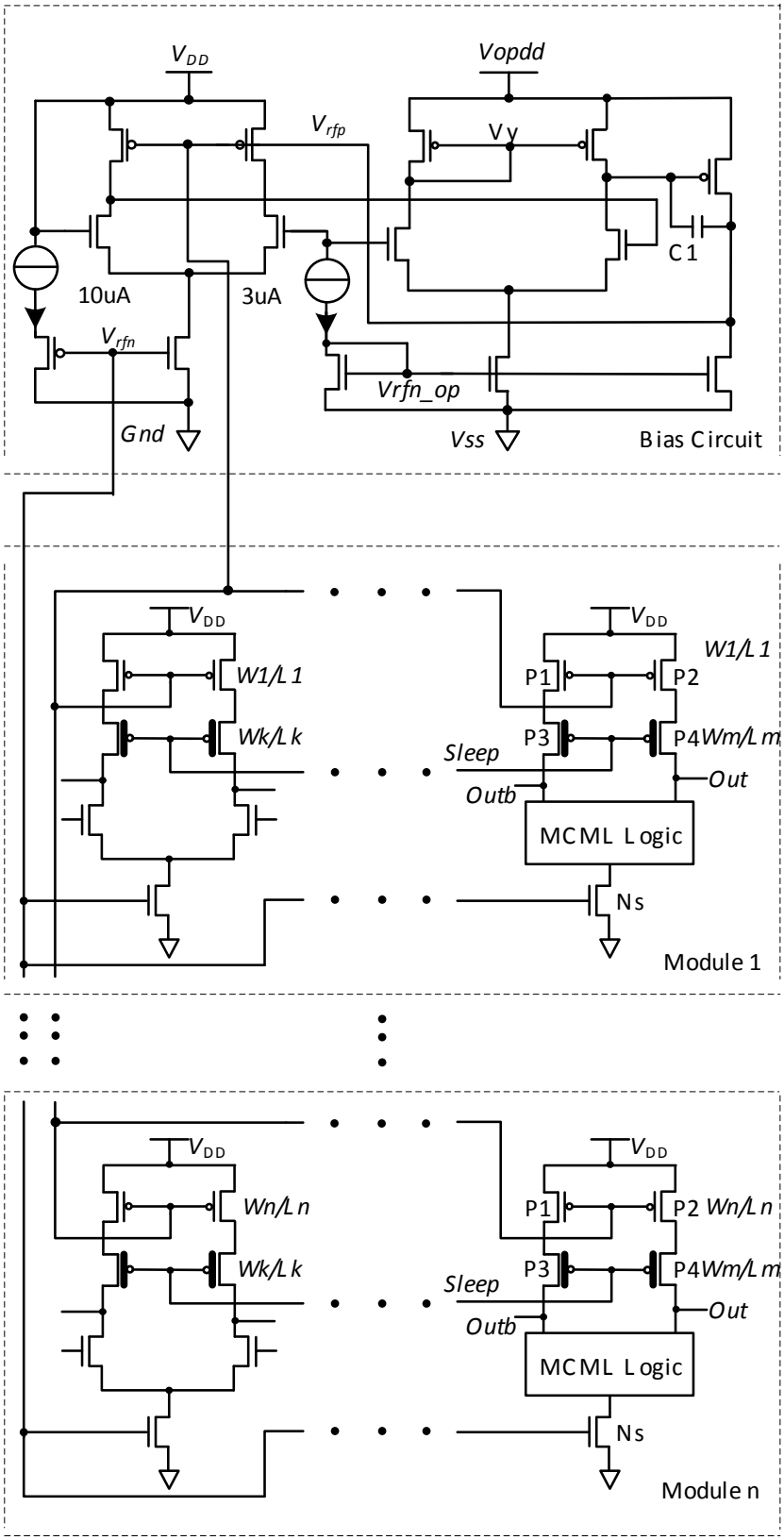

Fig. (3). The proposed power-gating MCML circuits where the widths and lengths of sleep transistors in power-gated blocks are separately adjusted.

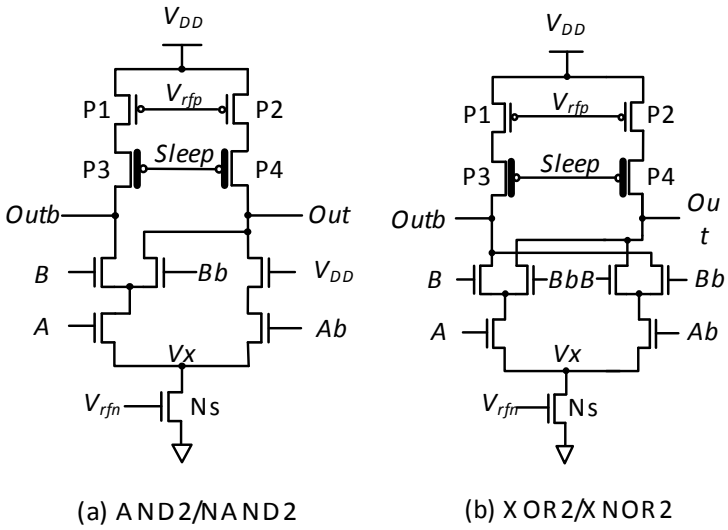

Fig. (4). Basic gates based on the proposed power-gating scheme.

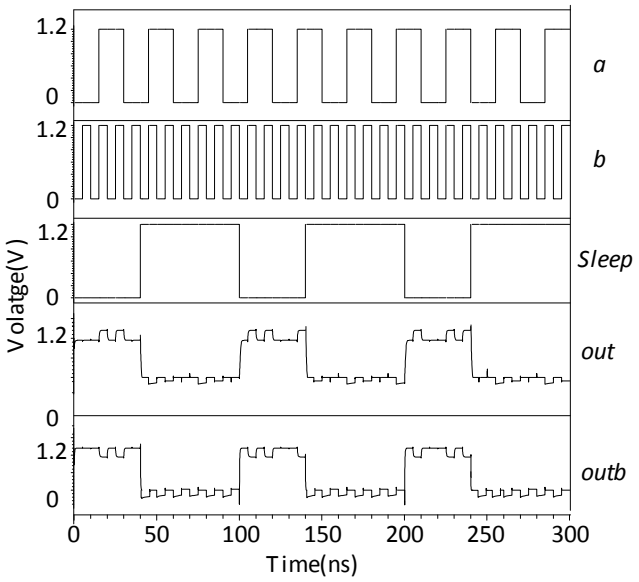

Fig. (5). Simulation waveforms of the proposed power-gating MCML AND2/NAND2.

control signal *Sleep* is 1, P3 and P4 are cut off, and the channel from V_{DD} to *GND* is shut down, so that circuit works in sleep mode. In this situation, the current from source voltage to ground do not exist, and thus energy consuming reduces dramatically.

In order to certify the correctness of proposed circuits, simulations have been made. All circuits are simulated by HSPICE with SMIC 130nm technology. The simulated waveforms of the power-gating MCML AND2/NAND2 that are based on the proposed scheme are shown in Fig. (**5**).

As is shown in Fig. (**5**), the circuit has proper functions. The work mode of circuits can be controlled by adjusting the value of *sleep*.

4. ENERGY DISSIPATIONS

In the MCML circuits that has separable power-gating scheme, the switches introduce an additional energy loss. In this part, the power-gating block with the power-gating switches and the no-power-gating block without the power-gating switches are considered. In the no-power-gating block, logic circuits are powered by the output of load transistors P1 and P2 for all the time (Fig. **1**).

One of the most important features in MCML circuits is that their energy dissipation is independent of frequency, and their value can be calculated by formula (3). Therefore, in No-power-gating MCML blocks, the energy loss can be acquired easily.

In active mode, the circuit of Fig. (**6a**) can be modeled as Fig. (**6b**). Since the current of NMOS transistor (NS) varies slightly as V_x changes because of the different state of the pull-down network and the different sizes of power-gating switches, the resistance R_{Ns} in the Fig. (**6**) is used to model this effect of the energy disoperation, which is converted to V_{DD}. Therefore, the energy dissipation in active mode can be expressed as

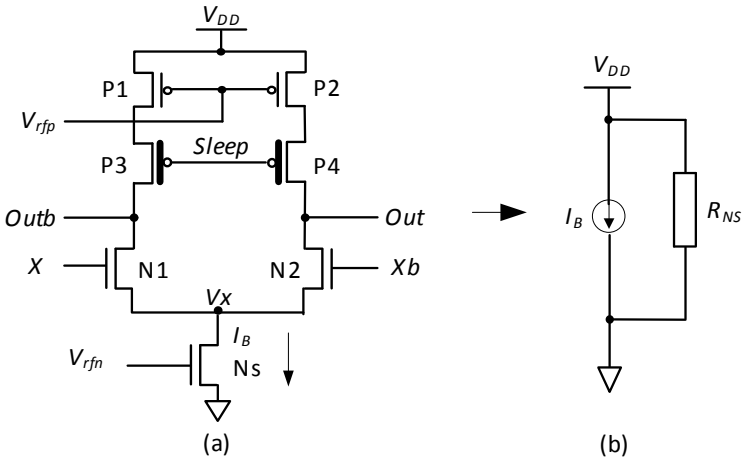

Fig. (6). Equivalent model when circuit works in active mode.

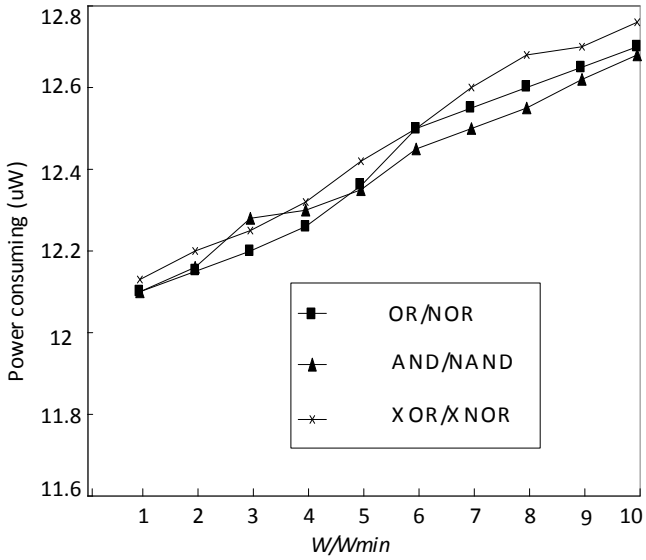

Fig. (7). Power consuming of the proposed power-gating MCML gates in active mode versus channel width of power-gating switches at 800MHz (W_{min} = 0.52μm, L = 0.65 μm).

$$E_{active} = V_{DD} I_S T_{active} + \frac{V_{DD}^2}{R_{NS}} T_{active} \tag{4}$$

Similarly, its power consuming is

$$P_{active} = V_{DD} I_S + \frac{V_{DD}^2}{R_{NS}} \tag{5}$$

Fig. (**7**) shows the power dissipation of the proposed power-gating MCML AND2/NAND2, OR/NOR and XOR/XNOR in active mode. From Fig. (**7**), the power dissipation only swings from 40.1μw to 40.7μw for the different sizes of power-gating switches. The simulation results show that the power dissipation is almost constant in active mode since the current of NMOS transistor (NS) varies only slightly as V_x changes. Take the error of experiment into consideration, a conclusion can be made that widths of power-gating transistors have little influence on the power consumption when the circuit operates in active mode.

In the sleep mode, the equivalent circuit of power-gating part can be modeled as Fig. (**8**).

In sleep mode, energy consuming still exist because of $I_{leakage}$ that means the leakage current of PMOS. The power dissipation can be expressed as

$$P_{sleep} = V_{DD} I_{leakage} \tag{6}$$

Where, V_{DD} is the source voltage and $I_{leakage}$ is the current mentioned above. The simulation result is shown in Fig. (**9**). The power consumption in sleep mode is much less than that in active mode.

In the sleep mode, the power consuming is almost the same for different gates. From Fig. (**9**), the energy dissipation of the power-gating circuit in sleep mode increases as the channel width of the power-gating transistor increases. P_{sleep} is almost independent of the bias current. These conclusions prove the correctness of the theories.

Average energy dissipation each cycle of power-gating circuits can be described as

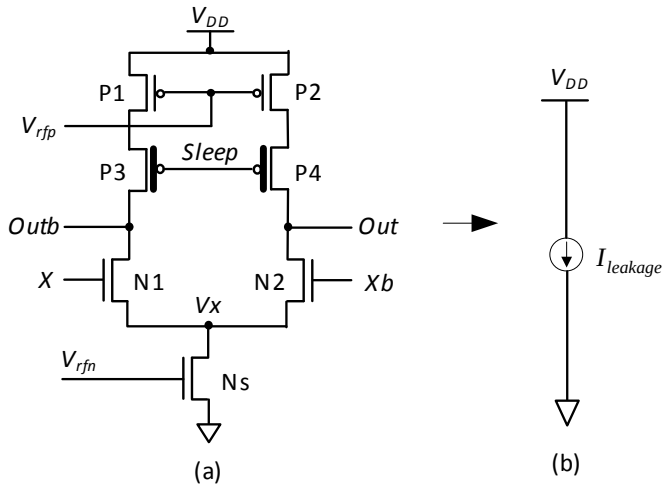

Fig. (8). Equivalent model when circuit works in sleep mode.

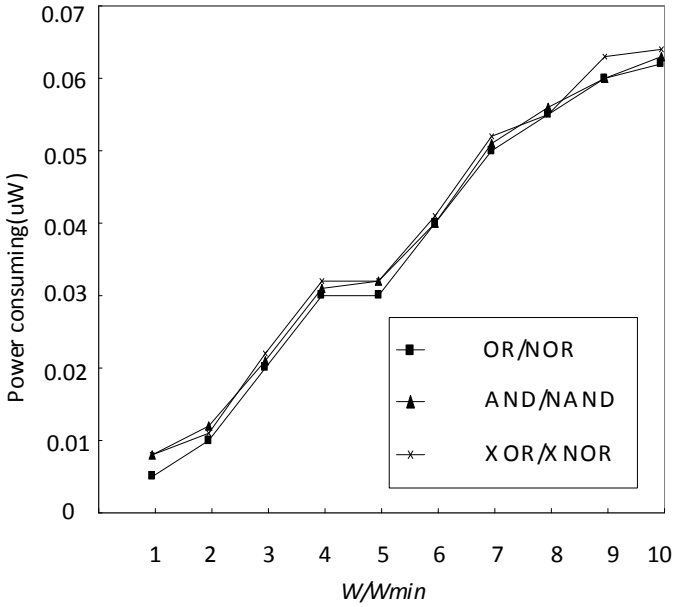

Fig. (9). Power consuming of the proposed power-gating MCML basic gates in sleep mode versus channel width of power-gating switches at 800MHz (W_{min}=0.52μm, L=0.65μm).

$$P_{AV} \approx (P_{active})\alpha + P_{sleep}(1-\alpha) \quad (7)$$

Where, $\alpha=T_{active}/(T_{active}+T_{sleep})$, which is the active ratio of power-gating. In order to certify whether the circuits are energy-sufficient or not, the contrast of power consumption between ordinary and the power-gating MCML 1-bit full adders that based on the proposed scheme is made. All the power dissipations represent the average power losses. The operating frequency is from 100MHz to 1GHz while the active ratio of power-gating circuit is 0.6. The outcome is shown in Fig. (**10**).

The power dissipation of power-gating MCML 1 bit full adder is 16.44uW, 16.74uW and16.97uW with the operating frequency of 100MHz, 500MHz and 1GHz, respectively. On the other hand, the power consumptions of ordinary MCML circuits are shown as 25.84uW, 25.86uW, and 25.85uW, respectively. The power-gating MCML circuit can nearly save 36% energy at an active ratio of 0.6.

As a new scheme, more contrast should be made to evaluate it objectively. In this work, static CMOS logic circuit is used to evaluate energy efficiency. Fig. (**11**) shows the power dissipation of these three logic circuits.

From Fig. (**11**), static CMOS logic circuit has lower power loss than MCML circuits when it operates in low frequency region, but its power consumption rises linearly with the increase of frequency. The power dissipations of the no-power-gating MCML 1 bit full adder and the power-gating MCML one are independent of frequency. Besides, the power consumption of power-gating MCML circuit (with an active ratio of 0.6) is 30% less than the no-power-gated one.

The comparison between power-gating MCML circuit and no-power-gating static CMOS logic one has been made

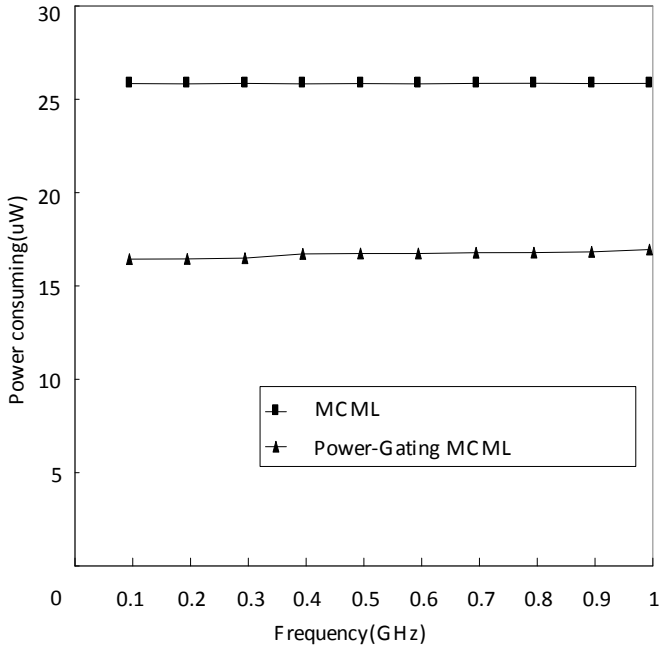

Fig. (10). Power consumption of conventional MCML 1 bit full adder and the power-gating 1-bit full adder that based on the proposed scheme with an active ratio of 0.6.

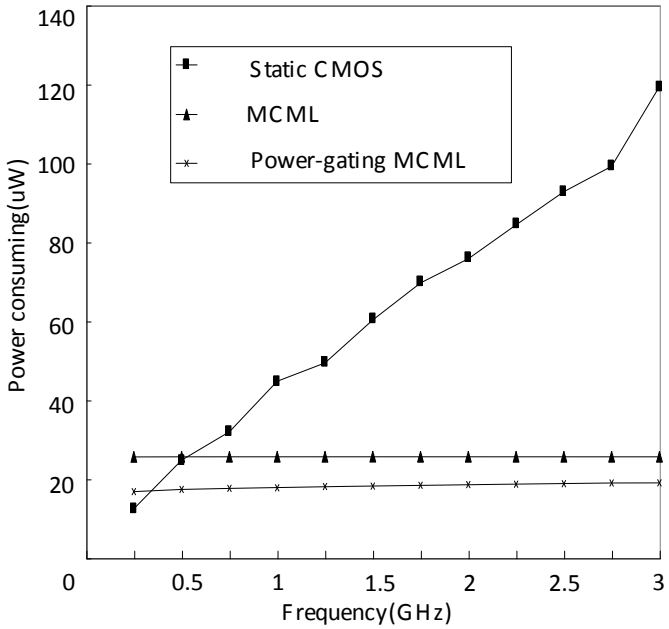

Fig. (11). Power dissipation of static CMOS logic, MCML and power-gating MCML 1 bit full adders (active ratio=0.6) with various frequencies.

in Fig. (**11**). However, this comparison is not comprehensive because the static CMOS logic circuit is no-power-gating circuit while the MCML circuit is a power-gated one. Therefore, another comparison between the power-gating static COMS logic circuit and the power-gating MCML one has also been made, as shown in Fig. (**12**). The simulating circuit is the 1 bit full adder, and operating frequency various from 250MHz to 3GHz with a rising step of 250MHz.

In Fig. (**12**), when operation frequency exceeds 750MHz, the circuit of power-gating static CMOS has a greater power consumption than the power-gating MCML one. Besides, the curve of power-gating static CMOS logic circuit rises linearly with the increase of frequency, and thus the gap of power-dissipation between the power-gating static CMOS logic circuit and the power-gated MCML one becomes greater when operation frequency is higher.

As a power-gating circuit, the active ratio α of power-gating is an important parameter. From (7), it is easy to

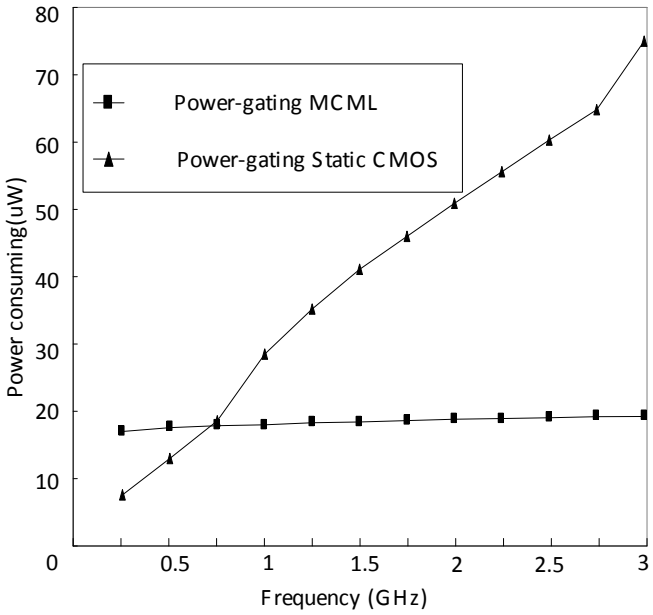

Fig. (12). Power dissipation of power-gating static CMOS logic and power-gating MCML 1 bit full adders (active ratio=0.6) with various frequencies.

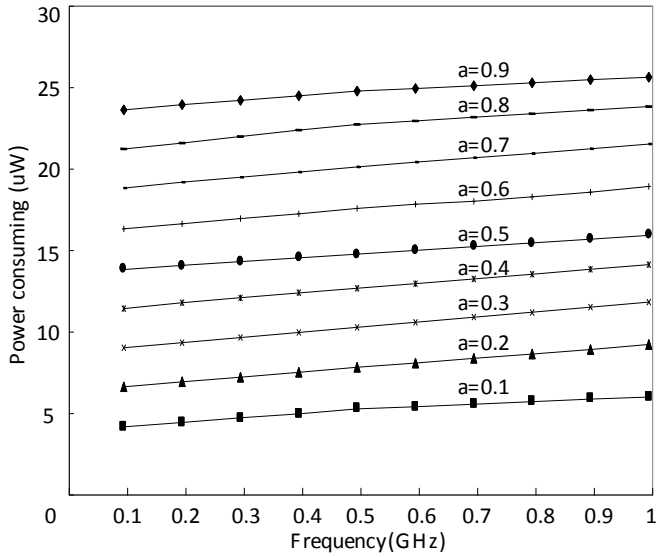

Fig. (13). Power consuming of proposed power-gating MCML 1 bit full adder with various active ratios.

know that the active ratio α has a great influence on the energy dissipation. Fig. (**13**) shows the effect of active ratio. It is the outcome of the power-gating MCML 1 bit full adder based on the proposed scheme with various active ratios from 100MHz to 1GHz with 100MHz step.

Power-consumption increases markedly with the rising of active ratio. It is easy to understand these phenomena because high active ratio means circuit works in active mode with a longer time compared to the circuit with low active ratio.

CONCLUSION

A power-gating scheme for MCML circuits with separable-sizing sleep transistors is proposed in this paper. In the proposed scheme, two high-threshold power-gating transistors are inserted between load transistors and outputs of the MCML circuits. The widths and lengths of sleep transistors in power-gated blocks are separately adjusted, which are independent of the bias circuit. Therefore, one bias circuit is enough for the power-gating MCML modules with different widths and lengths.

The HSPICE simulations certified the correctness of this scheme. The research for power dissipation is carried out. The 1-bit MCML full adder based on the proposed scheme nearly saves 36% of energy dissipations with respect to no-power-gating MCML one, for an operation activity of 0.6. Besides, the power consuming of the MCML 1-bit full adder based on the proposed scheme is 63.2%, 44.8%, and 36.97% compared with the power-gating static CMOS one when the

operating frequency is 1GHz, 1.5GHz, and 2GHz, respectively.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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