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The Open Electrical & Electronic Engineering Journal, **2014,** *8,* **77-83**

Open Access

Test Pattern Generation with Low Power for Delay Faults in Digital Circuits by Evolution Method with Hybrid Strategies

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Abstract: The high power consumption during circuit test process can produce unwanted failures or take effects on circuit reliability, therefore the reduction of both peak power and average power of circuit test is necessary. A test pattern generation approach is presented in this paper for the delay faults in digital circuits, the approach makes use of the evolution method with the hybrid strategies to produce the test vectors with low power consumption. First of all, a pair of vectors that may detect a delay fault is coded as an individual. A lot of individuals constitute the populations. Secondly, the test vectors with low power are produced by the evolution of these populations. Many new individuals are randomly produced and are added into every evolution step, and the mutation mode of individuals is related to other individuals in the current population. A lot of experimental results show that the test vectors with low power for the delay faults in digital circuits can be produced by the approach proposed in this paper, and the approach can get the large reduction of power consumption when compared with random test generation algorithm.

Keywords: Digital circuits, low power, test pattern generation, delay faults, evolution method.

1. INTRODUCTION

The major concerns of VLSI design are area, performance, reliability and power consumption. In recent years, the power consumption has received more and more attentions [1, 2]. The low power plays a significant role in the design of the high performance circuits such as microprocessors and other high-speed digital circuits, where the high clock frequencies are needed. The increase of power consumption is proportional to the rise in clock frequency. The power consumption of circuits is the dissipation in the form of heat, this heat may results in some problems such as the operating failures and the degradation of circuit performance [3, 4]. The portable electronics or mobile communication devices such as laptops and cellular phones etc. are the most important factor that drives the needs for the circuits with low power.

In general, for the functional operations of circuits, only a small percentage of nodes in the circuit have the transitions during a clock cycle, the reason is that only a small percentage of input values of these nodes will change while the rest of the input values keep their previous values [5]. For the test of circuits, the power consumption during test procedures is proportional to the frequency of the charging and discharging of the parasitic capacitances in a circuit component, therefore the power consumption is dependent on the number of signal transitions.

For example, if the scan architecture is used during circuit test, then the following test mode is employed: the test vectors are loaded into the scan architecture by shifting one bit of the test vectors per clock cycle into the scan chain, while the test responses from the previous test vectors are unloaded from the scan chain. The shifting procedure of the test data produces the large power consumption in the circuit. Hence, the large amount of test data causes the large power consumption during circuit test process, this type of power consumption will take effects on circuit reliability, sometimes, which may damage the circuit. Hence, it is necessary to design the test methods with low power.

For the patents of the test pattern generation with low power, a lot of approaches had been presented. For example, a structure of scan test circuits for the design of low power scan cell was given [6], the scan test circuit has at least one scan chain that can be used to configure the operations of the serial shift registers and to capture functional data from the circuits. The scan test with low power was investigated [7], the circuit structure contain a test stimuli selectors, scan enable circuits, clock enable circuits and shift enable circuits etc. , a test pattern generation method being proposed can be integrated with a lot of compression hardware architectures. The methods for the low power decompression of the test patterns were discussed [8], a low power test scheme that can reduce switching rates and the power dissipation was proposed, the scheme can be integrated with a variety of

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1874-1290/14

compression hardware architectures. The low-power built-in self-test was investigated [9], the test logic and a loading circuit that enable to load a shift test pattern were given, the shift test pattern may be configured to test the faults in the circuits. An approach of reducing the test operation power was proposed [10], the approach improved the scan test technique such that only portions of the scan circuit were activated at any one time.

At present, many aspects for the test pattern generation with low power have been investigated, such as, (1) The test pattern generation methods for low power. (2) The built in self test (BIST) with low power. (3) The low power test of system-on-chip. (4) The low power for scan-based test. (5) The test data compress for low power test. In the following, each aspect above is discussed in detail.

For the test pattern generation methods for low power, the main aims are to analyze the power being generated by test pattern, and how to produce the test pattern with low power by means of the circuit structure. Some method had been proposed for this, for example, the reduction in peak power of automatic test pattern generation (ATPG) for the *n*-detection test was investigated [11], and a power-aware test compaction method was discussed. The probabilistic and constraint based method was discussed for scan-based low power test generation [12], the signal probability analysis was used to estimate the fault detection probability and signal transition activities. The power consumption during test for scan-based circuit design was discussed [13], the approach that combines testability-aware test pattern generation with the scan chain disabling strategy was proposed, such that the non-used scan chains can be disabled during capture cycles. The partial gating of scan cells was investigated for reducing dynamic power dissipation during scan-based test [14], a systematic method was given for selecting the area and performance constraints to get the gating subset of scan cells, this method can reduce the average switching activity during test. The broadside templates was defined as the incompletely-specified broadside tests [15], which can capture the signal-transitions, a method of low power test generation was proposed by using the functional broadside templates.

About the built in self test (BIST) with low power, the BIST is a technique that designs additional hardware and software features into a circuit to allow performing self-testing. It is needed that the test patterns being produced by the test pattern generator in the BIST structure have low power.

A lot of methods had been proposed for this, for instance, a low hardware overhead test pattern generator for scan-based BIST was discussed [16], the generator can decrease the transitions that occur at scan inputs during scan shift operations, therefore can reduce the switching activity in the circuits under test. The adaptive low power random test pattern generator was discussed [17], which can improve the tradeoff between shift power reduction and the test coverage, the generator made that the previous test responses were given as feedback to a transition controller. A low power BIST architecture using pattern mapping strategy was investigated [18], the architecture made use of transition freezing approach that produces the frozen patterns according to the transition tendency of a linear feedback shift registers (LFSR), therefore the BIST architecture can get the average power reduction. A pseudorandom test pattern generator with pre-selected toggling activity for BIST was proposed [19], the generator was comprised of a linear finite state machine driving a phase shifter, and can produce binary sequences with low switching rates while can preserve the test coverage. The low power BIST for scan-shift was investigated [20], and a low power BIST approach was proposed, the approach can reduces shift-power by eliminating the specified high-frequency parts of vectors, and also can reduce the capture power.

About the low power test of system on chip (SoC), the SoC has a huge amount of test patterns, which results in great power consumption during test, it is needed to test SoC by using test patterns with low power.

Fox examples, an automatic test pattern generation (ATPG) approach based on functions was presented [21] for the test of the embedded cores, the approach can reduce both the test cost and the test power dissipation of SoC, the cores were tested concurrently by using the test functions and the I/O pin allocation on the test access mechanism. The test of power switches in SoC was discussed [22], a circuit structure and a method were given, which can perform the testing of on/off functionality for the power switches, the advantage of the method was that it only needs a small number of test patterns. The approach that can minimize the test time of SoC under the given power budget and varying test clock frequency for every test session was given [23], a test scheduling model was designed to include a variable frequency parameter that can controls the power and the test time. A test scheduling algorithm was presented to satisfy the resource, power, and thermal constraints [24]; the superposition principle was used to perform the thermal simulation, the algorithm can get the solutions of the test scheduling problem by introducing the cooling periods. For the power consumption in the SoC, a method of reducing peak current during scan based test was presented [25], the method modified the test compression logic to get that both the bypass scan chains and shift in constant values into the bypassed flip-flops can be implemented to reduce the instantaneous current.

About the low power for scan-based test, the main aims are to reduce the peak switching activity during shift and capture cycles in scan design. Several methods had been proposed for this.

For example, the approach for reducing the switching activities of power-risky patterns during the at-speed scan-based test was investigated [26], the approach consists of the test pattern refinement and low-power test pattern regeneration, the test patterns obtained using the proposed method are guaranteed to be power-safe for the given power constraints. A low power test scheme which is integrated with the embedded deterministic test environment was proposed [27], where a flexible test cube encoding scheme was used, the encoding scheme in conjunction with the continuous flow decompressor can reduce toggling rates when test patterns

are fed into scan chains. A scan architecture that can reduce the peak test power and capture power was presented [28], where a subset of scan flip-flops was activated to shift test data or capture test responses in any clock cycle. A design method of a scan flip-flop was proposed [29], which was able to eliminate the power consumption being produced by the unnecessary switches during scan shift, the scan flip-flop disables the slave latch, an alternate low cost dynamic latch was used. A segment-based filling method was proposed [30], which can be used to reduce the test power, the method used the configurations of the scan chains, where all the bits of some scan chains in a vector may be don't care. The low-power test of the compression-based reconfigurable scan architectures was discussed [31], it was shown that the distribution of care bits in scan chains can produce the effects for the peak and average power of the reconfigurable scan.

About the test data compress for low power test, it is an effective solution to the problem of increasing test data volume. In general, there is an on-chip decompressor, which decompresses the data as the test patterns that can be applied the circuit under test, therefore it is necessary to consider the compress of test patterns such that the test patterns obtained by decompressor have low power.

For instance, the method for the input test data compaction and scan power reduction was investigated [32], an approach was given to hold values if it is not necessary to change the test data in test cubes. The compression rate of a given test set can be improved by organizing the test data being presented in scan structure [33], the theoretical maximal compression can be increased by the scan flip-flops partitions such that there is skewed signal distribution for the test data being presented in each partition. The low power test method can be integrated with the embedded deterministic test environment [34], the switching rates in the scan chains can be reduced by using the method, and that it can obtain the minimal modification for the scan chains. The mathematical models of compression ratio was investigated [35], a test decompression scheme was proposed for the single test input, the aim of the encoding scheme is to maximize the number of duplications that have been produced by the test-slice templates. The low-power test approach can be compatible with the test compression environment [36], the flexible test application scheme can be obtained, the switching activity during the phases of scan test can be reduced, such as the loading, capture, and unloading phase.

In this paper, a new test pattern generation approach with low power is presented for the delay faults in digital circuits, the approach makes use of the evolution method with the hybrid strategies.

2. TEST OF DELAY FAULTS

The timing is becoming more and more important with the increasing speed of circuits and the advances in the circuit fabrication technology. A lot of defects may be introduced in the fabrication procedure of circuits. The defects can cause a circuit work incorrectly, for example, some of the defects can cause functional failure, and other defects can influence the circuit speed or the timing behavior, therefore the defects may reduce the total performance of circuit.

In general, in the normal circuit design, each gate in a circuit has a specified rise or fall delay from its input lines to output lines, and the interconnection lines in the circuit are assumed to have specific rise or fall delays. There are a number of defects that can cause delay faults, such as the resistive shorting defects between the signal lines and the supply rails, the parasitic transistor leakages, the incorrect or shifted threshold voltages, certain types of opens, etc. The delay faults or timing related faults may cause the incorrect delay on a gate or on a path in a circuit. For the synchronous circuits, the delay faults may cause the circuit to be activated at a slower rate. For the asynchronous circuits, the delay faults may cause incorrect operations of circuit.

The delay faults are divided into two types: gate delay faults and path delay faults. The gate delay faults assume that the delay fault be lumped at one gate in circuit. A transition signal that propagates through this gate will be delayed, and may produce incorrect values at the primary output of circuit. The effects of delay in one or more gates in the circuit are considered, and these delays in gates may also cause an increased delay in the circuit output.

The transition fault model is one of the most popular gate delay faults. In this transition fault model, every signal line in the circuit may be associated with the following two faults: the slow-to-fall faults and the slow-to-rise faults. The slow-to-fall transition faults produce the extra delay for a falling transition on a line, and the delay of each path through the line exceeds the timing constraints being given by the design specifications. Similarly, the slow-to-rise transition faults produce the extra delay for the rising transition on a line in the circuit. The transition fault model has a following feature: The number of delay faults is linear in the number of the signal lines.

A physical path is defined as an interconnection of gates from a primary input to an observation node (e. g. a primary output line of circuit). There are two following logical paths being associated with a given physical path: the rising path and the falling path. The rising path is the path traversed by a transition that is applying a rising transition at the input of the physical path. The falling path is the path traversed by a falling transition. The path propagation delay is the time that takes a transition to propagate through a logic path.

The path delay faults consider the delay faults on paths from primary inputs to primary outputs in a circuit. A path delay fault is said to have occurred if the delay of a path exceeds the specified clock period of the circuit, where the effect of delay fault in one path is considered, and the effect in the path increases the output delay of circuit.

When the changes in the delay values of several gates or interconnect lines are small, the changes in delay values of these gates and interconnects lines along some path may cause the path delay to exceed the desired clock period. Therefore, the path delay faults are more suitable for tackling delay faults since they can model a larger set of faults. In this paper, the path delay faults are considered.

The test of delay faults can be applied to detect timing defects, the small distributed defects and the failures due to excessive process variations. The test of delay faults can ensure that the fabricated circuit meets pre-specified timing

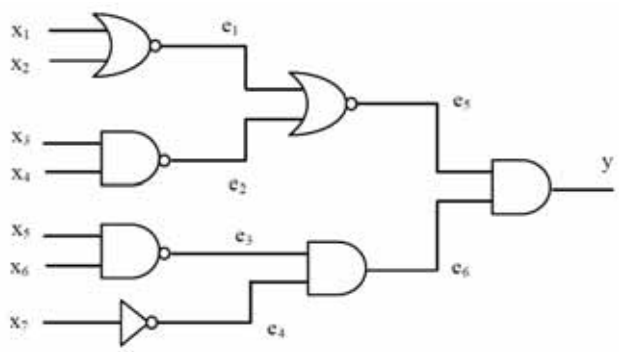

Fig. (1). A circuit for delay fault.

specifications. For the modern digital circuits, the test of delay faults is becoming more and more important due to the rapidly shrinking process feature size and the increasing operation speed. For instance, some of processors have the clock speeds of more than 1GHz, and the timing variation tolerance is under a few picoseconds.

The procedure for the test of delay faults is to propagate a transition through a path from a start node to an end node, this can be accomplished by using two clock pulses: a launch clock pulse and a capture clock pulse, where the first clock pulse launches the transition, and the second clock pulse captures the transition.

It is necessary a pair of vectors v_1 and v_2 for the test of a delay fault, the v_1 is required to initialize the target nodes (signal lines), the v_2 is required to launch the appropriate transition at the target nodes, and propagate the transition to an observation nodes such as the primary outputs of circuit. Therefore, the test vectors of delay faults can create a desired transition at the primary inputs of circuit, and can propagates the transition through the fault location and to a primary output of circuit. An example for the test of delay fault is shown in the Fig. (**1**).

For example, if there is a delay fault on the path $x_4 - e_2 - e_5 - y$ in the Fig. (**1**). , then the first vector (named as v_1) that can sensitizes the path, and enables the propagation of one transition from line x_4 to line y by making all the gates in this path transparent. Here, the first vector v_1 can be chosen as $v_1=(x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7)$ =(0 0 1 0 1 1 0). Afterwards, a signal change in the line x_4 at the time *t* is forced, therefore the second vector (named as v_2) is needed, $v_2=(x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7)$ =(0 0 1 1 1 1 0). This results in that the transition time at circuit output y is measured, which will occur at a time ($t + T_0$). If the transition delay T_0 is outside the margin being defined in advance, then there is a delay fault on the path $x_4 - e_2 - e_5 - y$. Thus, the vector $v=(v_1, v_2)$ can detect the delay fault on the path. Similarly, the vector $v=(v_1, v_2)$, v_1=(0 0 0 1 1 0 0) and v_2=(0 0 0 1 1 1 0), can detect the delay fault on the path $x_6 - e_3 - e_6 - y$.

3. TEST PATTERN GENERATION WITH LOW POWER FOR DELAY FAULTS

The power consumption is becoming a major aspect of VLSI circuit design. The power consumption is being given comparable weight to the area and the speed of circuits, it determines the packing mode, the thermal and electrical limits of components in the circuit. There are following four aspects that cause the power consumption in the CMOS digital circuits.

(1) Capacitance current. It flows to charge and discharge capacitive loads during logic changes. For example, during the discharging process of a capacitance in a circuit, the energy that is stored in the output capacitor gets dissipated through a number of transistors and the interconnection lines.

(2) Short-circuit current. It is due to the direct supply-to-ground connections that are created during signal transitions. The powers being caused by short-circuit current are related to the sizing of transistors, the scale of the supply voltage, and the switching activity at the outputs of gates.

(3) Leakage current. It is determined primarily by the circuit fabrication technology, for example, it is due to the sub-threshold leakage current and the reverse biased diode current. The sub-threshold leakage current is produced by means of that the transistors conduct some current even when they are idle. The reverse biased diode current is produced among a number of the diffusion regions and the substrate.

(4) Standby current. It is the current drawn continuously from the supply voltage V_{dd} to the ground, i. e. , it is the current that the circuit draws when the circuit is not actively performing its function.

The power consumption can also be divided into following two types: static power and dynamic power. The dynamic power *Q* is dominant in total power consumption, it is the charging and discharging of the node capacitances, and can be expressed by the following equation.

$$Q = 0.5 \cdot C_L \cdot V_{dd}^2 \cdot E_s \cdot f_c \quad (1)$$

The C_L is the physical capacitance at the output of the gate, the V_{dd} is the supply voltage. The f_c is the clock frequency. The E_s is the average number of output transitions per $1/f_c$ time. The product of E_s and f_c is the transition density.

Several different means can be used to reduce the power consumption according to the equation (1). For example, these means include the reduction of load capacitance C_L, the reduction of power supply voltage V_{dd}, the reduction of the clock frequency, and the reduction of the number of transitions, etc. Here, the reduction of transitions (i. e. , switching activity) requires the detail analysis of signal transition probabilities.

The impacts of power consumptions during test process has been analyzed, the results show that the power consumption during test process tends to be significantly higher than that the power consumption during the normal mode of the operation of circuits. Therefore, the power consumption (especially the peak power consumption) during test process must be kept under a defined value. The excessive peak power during test process may cause an increased big current

flow in the circuit under test, which can lead to electromigration, or produce unwanted failures, and reduce the circuit reliability and lifespan.

Therefore, it is necessary to perform the reduction of power consumption in the circuit test. In this paper, for a given circuit, the power consumption *P* (during the test vectors are applied to the primary inputs of the circuit) is expressed by the equation:

$$P = \frac{1}{2} \cdot C_L \cdot V_{dd}^2 \cdot f_c \cdot \sum_{i=1}^{G} \sum_{j=1}^{H} a(j) \quad (2)$$

Where the *G* is the number of test vectors, the *H* is the number of the gates in the circuit, the $a(j)$ is the switching activity factor of the output of the gate *j*.

In the following, a test generation approach is presented for the test of delay faults, the approach uses the evolution method with the hybrid strategies to generate the test vectors with low power consumption for the delay faults in digital circuits. In this evolution method with hybrid strategies, a lot of new individuals are randomly produced and are added into every generation population, and the mutation mode of individuals is related to other individuals in current population. The implementation steps of the test generation approach are given in the following Algorithm 1.

4. ALGORITHM 1

Step 1. Set parameter t=0, set the value of the *N* that is the number of the individuals in a population.

Step 2. Randomly produce an initial population U(0) that is consisting of the *N* individuals.

Step 3. For each individual in the population U(t), perform the fault simulation by using the individual, and compute the power *P* of the individual by the equation (2). The fitness of each individual is defined by the expression $1/(P+0.05)$.

Step 4. Carry out the operations of selection and crossover for the individuals in current population U(t). Here, the roulette wheel selection and two points crossover are used. The individual is selected on the basis of fitness in the roulette wheel selection, the probability of an individual to be selected increases with the fitness of the individual.

In the two points crossover, firstly the two points are selected randomly on the parent individuals, secondly everything between the two points is swapped between the parent individuals to constitute new child individuals.

Step 5. Perform the mutation operations for a lot of the individuals in the current population U(t). First of all, choose some individuals from the population U(t) by using the probability P_m, here suppose the number of individuals being chosen is *K*.

Secondly, make one position (which is selected randomly, e. g. , the j-th component) of every individual that belongs to the chosen *K* individuals to change its value, the approach is as follows. Define folllowing three modes:

The mode 1: Randomly choose *M* individuals from the population U(t).

The mode 2: Randomly choose *M* individuals, where the fitness of each such individual is higher than the average fitness of the individuals in the population U(t).

The mode 3: Randomly choose *M* individuals, where the fitness of each such individual is lower than the average fitness of the individuals in the population U(t).

For an individual ξ that belongs to the chosen *K* individuals, perform the following operations: (1) Generate a random number *d* that belongs to [0, 1]. The model 1 is selected if the $d \leq 0.5$; The model 2 is selected if the $0.5 < d \leq 0.75$; The model 3 is selected if the $0.75 < d \leq 1$. (2) Compute the average value *w* of the j-th components in the chosen *M* individuals obtained by one of the above three modes. If the value of the *w* is greater than 0. 5, then the value of the j-th component of the individual ξ is 1, else the value is 0.

Step 6. For the current population, randomly choose λ individuals and discard them. After words, randomly produce λ new individuals and add them into the current population.

Step 7. If the stopping conditions are satisfied, then stop the algorithm, otherwise, set t: = (t+1), go to Step 3.

In the Algorithm 1, the coding of an individual is as follows. An individual is a pair of vectors v_1 and v_2, which is corresponding to a test vector of a delay fault. If the number of circuit primary inputs is *n*, then the individual can be represented by a binary string $(z_1 z_2 \cdots z_{2n})$, where the $z_i=0$ or 1 for $i=1, 2, 3, \cdots, 2n$.

In the Step 5 of the Algorithm 1, the parameter *K* is determined by both the *N* and the probability P_m, in general, it is much less the value of the *N*.

In the Step 6 of the Algorithm 1, the parameter λ being chosen should much less than the value of the *N*.

5. EXPERIMENTAL RESULTS

The approach proposed in this paper has been implemented in C++ language for the test pattern generation with low power for the delay faults in digital circuits. The approach has been applied to the generation of test vector of delay faults for many digital circuits. A lot of experiments have been performed on a personal computer with 3. 0GHz and 1GB main memory under Windows operation system.

The ISCAS'89 benchmark circuits are used in these experiments. The ISCAS'89 circuits are sequential circuits described at the gate level, they can be used to evaluate the test pattern generation algorithm not only for full scan-based algorithm but also for partial scan-based algorithm. Besides, the ISCAS'89 circuits also can be used to identify the advantages and limitations for a sequential test algorithm. The structures of these circuits are shown in the Table **1** and Table **2**.

Table 1. The ISCAS'89 benchmark circuits.

Circuits	s344	s349	s382	s526	s820	s832
PI	9	9	3	3	18	18
PO	11	11	6	6	19	19
FF	15	15	21	21	5	5

Table 2. The ISCAS'89 benchmark circuits.

Circuits	s1488	s1494	s5378	s35932
PI	8	8	35	35
PO	19	19	49	320
FF	6	6	179	1728

In the Table **1** and Table **2**, the row "Circuits" represents the name of a benchmark circuit. The row "PI" shows the number of primary inputs in a benchmark circuit, the row "PO" shows the number of primary outputs. The row "FF" represents the number of flip-flops in a benchmark circuit. In the Table **1**, there are two circuits that have the same numbers of primary inputs, primary outputs and flip-flops, such as the circuit s344 and s349, but the structures of the two circuits are different. For example, the numbers of gates in the two circuits are not equivalent.

The parameters being used in the Algorithm 1 are as follows. The stopping conditions of the Algorithm 1 is defined by the following mode: The maximal number of evolution generations is reached, or the maximal fitness and average fitness do not change in the successive two generation populations U(t) and U(t+1). The maximal number of evolution generations is set as 2000. The value of parameter N is set as 34, the value of parameter λ is set as (N/10), i. e. , λ=(N/10). The crossover rate is 0. 94; mutation rate is 0. 01.

For the test pattern generation with low power, we have also carried out the other experiments by using random test generation algorithm. In this random test generation algorithm being used, the circuit input vectors are produced by randomly assigning a value 0 or 1 to each primary input of circuits. If the input vector being produced is able to detect a delay fault in the circuit, then the vector is selected as a test vector.

In these experiments, the following two stages are performed. Stage 1: the test set of each ISCAS'89 benchmark circuit is produced by using the Algorithm 1 or the random test generation algorithm. Stage 2: the test sets having obtained in the Stage 1 are applied to the primary inputs of the circuits to detect the delay faults and to get the power consumption of test vectors.

The experimental results show that the Algorithm 1 in this paper can produce the test set for each ISCAS'89 benchmark circuit in the Table **1** and Table **2**. The power consumptions of the test sets obtained by the Algorithm 1 are lower than the test sets obtained by the random test generation algorithm. The Algorithm 1 obtains the reduction value of power consumption that are ranging from 26% to 48% when compared with the random test generation algorithm. The reduction of power consumption is 26%, 30%, 28%, 37%, 35%, 39%, 32%, 36%, 48% and 44% for the circuits s344, s349, s382, s526, s820, s832, s1488, s1494, s5378, and s35932, respectively.

Summarize these experimental results, it is shown that the test generation approach proposed in this paper can obtain the test vectors with low power for the delay faults in digital circuits. Besides, because a pair of vectors v_1 and v_2 is needed for the test of a delay fault, therefore firstly produce the vectors v_1, then how to utilize the information of the vectors v_1 to produce the second vector v_2 in terms of the constraints of low power, this is valuable to deeply investigate in the future.

6. CURRENT & FUTURE DEVELOPMENTS

As the VLSI circuit design sizes and the operating frequencies continue to increase, the timing-related defects such as delay faults are high proportion of the total circuit defects. The power constraints that are defined for the circuit normal operations may be much lower than the power consumption during the circuit test mode. The large power consumption during test process may damage the circuit under test. In this paper, a test generation approach is presented for the test of the delay faults in digital circuits, the approach makes use of the evolution method with the hybrid strategies to produce the test vectors with low power. In the future, some work needs to be done for the better selection of the fitness functions being related to the low power in this approach.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

ACKNOWLEDGEMENTS

This work were supported by National Natural Science Foundation of China (No. 61072028, 61108039), the Project

of Department of the Education of Guangdong Province (No. 2012KJCX0040).

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Received: June 09, 2014 Revised: June 22, 2014 Accepted: July 24, 2014