Review on Optimization Methods of Carbon Nanotube Field-Effect Transistors

Changxin Chen* and Yafei Zhang*

National Key Laboratory of Nano/Micro Fabrication Technology, Key Laboratory for Thin Film and Microfabrication of Ministry of Education, Institute of Micro and Nano Science and Technology, Shanghai Jiao Tong University, Shanghai 200030, P.R. China

Abstract: Carbon nanotube field-effect transistors (CNTFETs) have been considered as a replacement for, or complement to, future semiconductor devices due to high mobility, low defect structure, and intrinsic nanometer scale of carbon nanotubes (CNTs). The great superiority in performance for CNTFETs *vis-a-vis* state-of-the-art silicon devices has attracted an intense research effort to explore their application viability. Since the first CNTFET was fabricated, CNTFETs have experienced great advances at the device structure as well as device performance. Various methods had been attempted to optimize the devices. These methods can mainly be divided into four aspects: (1) Decrease the contact resistance between CNTs and metal electrodes; (2) Increase the tuning efficiency of gate voltage to CNT channels; (3) Shorten the CNT channel length; (4) Adopt the optimized device structure. This review will briefly summarize these methods and describe the device performances achieved with these methods. Representative researches and updated progress on the optimization methods of CNTFETs will be introduced. From the review, the advances in CNTFETs can be also learned in the rough.

INTRODUCTION

An intense research effort into the viability of utilizing carbon nanotube field-effect transistors (CNTFETs) as a replacement for, or complement to, future semiconductor devices had been devoted due to high mobility, low defect structure, and intrinsic nanometer scale of carbon nanotubes (CNTs) [1-7]. CNTFETs have shown their great superiority in performance *vis-a-vis* state-of-the-art silicon devices. They are expected as one of the most promising technologies that might someday pick up where conventional CMOS devices leave off. The CNT-based electronics industry could not only preserve a lot of advantages for existing silicon technology but also solve the majority of problems that would probably prevent the achievement of extremely small CMOS devices [8].

The CNTFET was fabricated successfully for the first time in 1998 [9]. In this CNTFET, an individual semiconducting single-wall carbon nanotube (SWCNT) bridged two platinum source and drain electrodes patterned on the silicon substrate which was thermally coated by a thick (300 nm) silicon oxide layer (Fig. **1**). IThe transistor current could be tuned by applying a gate voltage to the silicon back gate to control the Schottky barrier between SWCNT and metal electrodes. So far, the CNTFETs has experience a great research progress on device structures as well as device performances. Various methods have been attempted to achieve the high-performance CNTFETs. In this paper, we will review and summary these methods at the following four aspects.

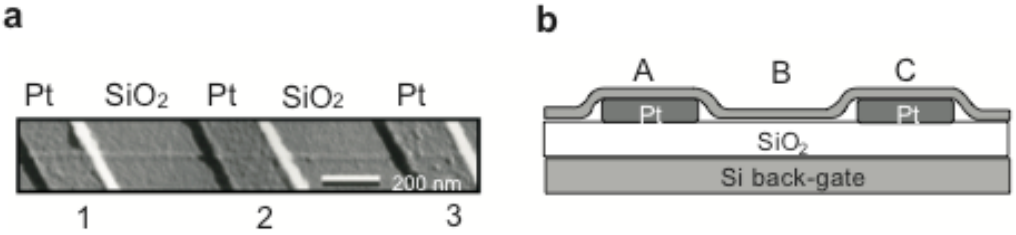

Fig. (1). (**a**) Tapping-mode AFM image of an individual carbon nanotube on top of three Pt electrodes; (**b**) Schematic side view of the TUBEFET device. Images adapted from reference [9].

THE METHODS TO IMPROVE THE DEVICE PERFORMANCE OF CNTFETs

Decrease the Contact Resistance Between SWCNTs and Metal Electrodes

When SWCNTs are placed on the metal electrodes, SWCNTs are contacted to electrodes by the weak van der Waals force, which causes a large contact resistance between SWCNTs and electrodes so as to degrade the device performance. Many ways had been attempted to decrease the contact resistance. R. Martel *et al*. adopted a high-temperature anneal method to improve the contact [10]. They fabricated the metal electrodes on two ends of SWCNTs and

*Address correspondence to either author at the National Key Laboratory of Nano/Micro Fabrication Technology, Key Laboratory for Thin Film and Microfabrication of Ministry of Education, Institute of Micro and Nano Science and Technology, Shanghai Jiao Tong University, Shanghai 200030, P.R. China;
E-mails: chen.c.x@263.net; chen.c.x@sjtu.edu.cn or yfzhang@sjtu.edu.cn

1874-1401/07 $50.00+.00

then annealed the devices at a high temperature (~800°C), which makes the SWCNTs and metal electrodes form the compound. With the high temperature treatment, the contact resistance could be decrease to ~30KΩ, the device current increased from the nano-ampere level to the micro-ampere level, and the transconductance (g_m~0.34μS) was enhanced by 200 times. C. W. Zhou *et al*. grew the individual semiconducting SWCNT between source and drain electrodes by CVD method and then fabricated the metal electrodes on SWCNTs [11]. The fabricated CNTFETs exhibited a transconductance of 200 nS and a gain of 3. In addition, the low-resistance contacts can also be obtained by choosing the suitable metal as contact electrodes. Au is found to be able to form the reliable and good contacts with SWCNTs [12] And Pd and semiconducting SWCNTs can form the Ohmic contact, which decreases the contact resistance significantly [13, 14].

Recently, a breakthrough to improve the contact of SWCNTs and metal electrodes has been acquired by our research group. An ultrasonic nanowelding technique has been developed for bonding SWNTs onto metal electrodes [15-17]. The nanowelding was formed by pressing SWCNTs against the electrodes with a welding head of Al_2O_3 crystal vibrating at ultrasonic frequency, as shown in Fig. (**2**). The welding surfaces with a diameter ranging from tens of to hundreds of micrometers were used in the nanowelding.

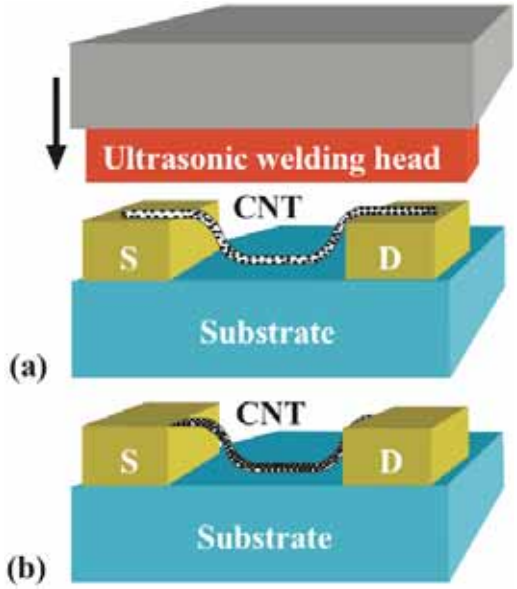

Fig. (2). Schematics of the ultrasonic nanowelding process. (**a**) before welding; (**b**) after welding. Images adapted from reference [15].

With this technology, firm and low-resistance contacts were achieved between both metallic and semiconducting SWCNTs and electrodes (Fig. **3a**). The device performances of CNTFETs fabricated with this technology had also been greatly improved (Fig. **3b**). A transconductance as high as 3.6 μS was achieved for the back-gate individual nanotube FETs.

Increase the Tuning Efficiency of Gate Voltage to SWCNT Channels

Another important method to improve the performace of CNTFETs is increasing the tuning efficiency of gate voltage to SWCNT channels. At present, there are mainly three ways to enhance the gate tuning efficiency.

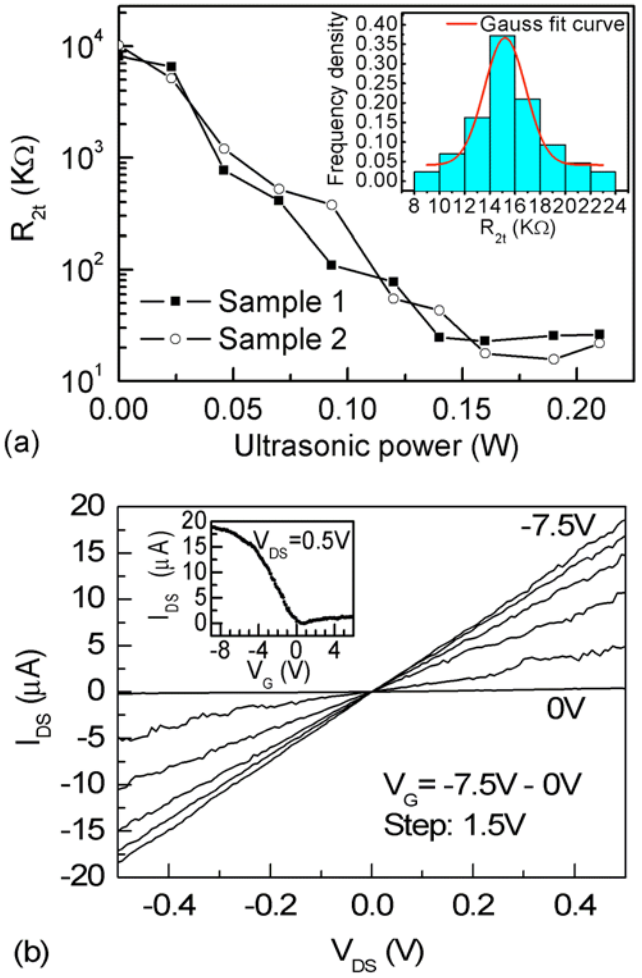

Fig. (3). Electrical performances of individual metallic and semiconducting SWCNTs after the ultrasonic nanowelding. (**a**) Two terminal (2t-) resistances as a function of the ultrasonic power for two metallic nanotube-Ti contacts. Before the ultrasonic nanowelding, the 2t-resistances of sample 1 and 2 were 49.4MΩ and 55.8MΩ, respectively; The ultrasonic power of 0 W in the figure represents the ends of the SWNT were pressed against the electrodes by pure clamping force without ultrasonic power applied. Inset: the statistical analysis and distribution fit of the obtained lowest 2t-resistances for 43 samples after nanowelding. (**b**) Output characteristic of the CNTFET with individual semiconducting SWNT as conduction channel. Inset: transfer characteristic curve. Images adapted from reference [15].

Use the Top-Gate Structure

For previous back-gate CNTFETs, a thick gate insulator (100-150 nm) was used, which generally cause a large threshold voltage. Moreover, the SWCNTs in the back-gate devices were exposed to air and the gate capacitance was diluted by the air with the low dielectric constant, which cause poor tuning efficiency for gate bias. In addition, each CNTFETs on the chip cannot be controlled separately for the back-gate structure. To solve the disadvantages, S. J. Wind *et al*. developed a top-gate CNTFET (Fig. **4**) [18]. At first, they fabricated the source and drain electrodes on two ends of SWCNT. Then, a gate dielectric was deposited from a

mixture of SiH_4 and O_2 by CVD method on the SWCNT. Finally, a Ti or Al electrode was overlaid on the SWCNT channel. It was demonstrated that the top-gate structure effectively enhances the tuning effect of gate bias. The threshold voltage of the device (-0.5V) is far lower than that (-12V) of back-gate device, the drive current and transconductance (g_m~0.34μS) were also increased effectively.

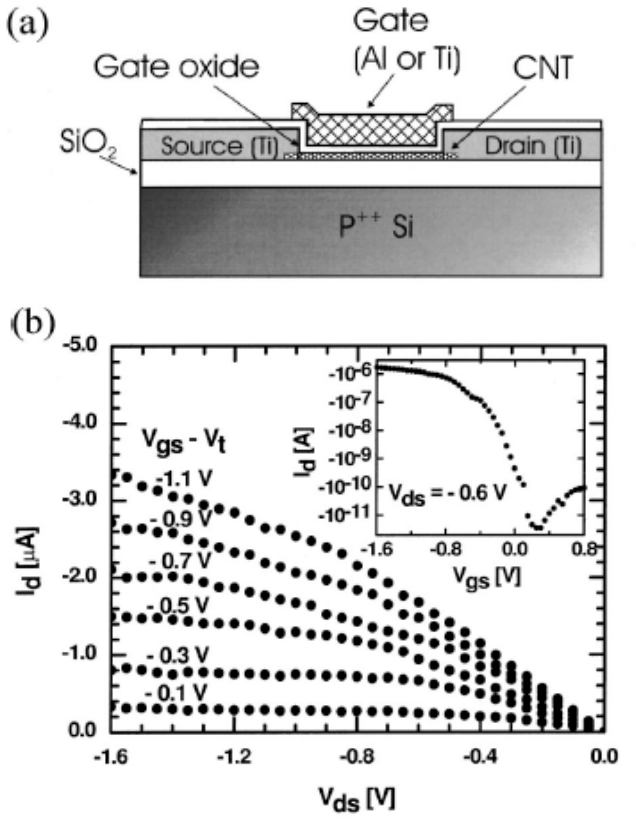

Fig. (4). (**a**) Schematic cross section of top gate CNTFET showing the gate and source and drain electrodes. (**b**) Output characteristic of a top gate *p*-type CNFET with a Ti gate and a gate oxide thickness of 15 nm. The gate voltage values range from -0.1 to -1.1 V above the threshold voltage, which is -0.5 V. Inset: Transfer characteristic of the CNTFET for V_{ds} =-0.6 V. Images adapted from reference [18].

Decrease the Thickness of Gate Insulator

Decreasing the distance of gate electrode and SWCNT can also increase the gate capacitance and thereby enhance the tuning effect of gate electrode. Though the principle for this way is relatively simple, the process is not easy to realize. A. Bachtold *et al*. successfully fabricated the CNTFET with a few nanometers-thick gate insulator [19]. They utilized a naturally oxided Al_2O_3 layer on the Al electrode as the gate insulator, whose thickness is estimated to be a few nanometers. The fabricated CNTFETs exhibited a transconductance of 0.3μS, an On-state current of ~100 nA, a gain of >10, and a current On/Off ratio of 10^5. Y. R. Lu *et al*. had fabricated the top-gate CNTFETs with the ultrathin high *k* dielectrics by depositing the HfO_2 on DNA-functionalized SWCNTs with atomic layer deposition (ALD) technique (Fig. **5**) [20]. With the DNA functionalization, the high performance nanotube-high *k* FETs free of gate-leakage currents were reliably obtained with HfO_2 thickness down to 2-3 nm. The fabricated CNTFETs could reliably achieving the subthreshold slope *S*=60 mV/decade at room temperature.

Adopt the High-k Gate Insulator

For the traditional MOSFETs, the gate capacitance C_G and gate insulator thickness t_{ox} have a relation of $C_G \propto 1/t_{ox}$. Different from the MOSFET, the gate capacitance of the CNTFET can be expressed as $C_G \approx 2\pi\varepsilon\varepsilon_0/\ln(2h/r)$, where ε, h and r are the dielectric constant, thickness of silicon dioxide, and the radius of the carbon nanotube, respectively. This slowly logarithmic dependence between the C_G and h for the CNTFETs degrades the effect of reducing the gate insulator thickness. Moreover, the too thin gate insulator will cause the unexpected bipolar characteristics. Therefore, ones begin appealing to high-*k* gate dielectric for increasing the gate capacitance.

J. Appenzeller *et al*. used HfO_2 (*k*~11) to displace SiO_2 as the gate insulator to fabricate the back-gate CNTFETs [21]. The 20-nm-thick HfO_2 layer was deposited on the n-type Si substrate by CVD method under 400ºC. The fabricated CNTFETs exhibit a drive current of 270 μA/μm, a maximum transconductance of 425μS/μm and an inverse subthreshold slope of 140 mV/dec. A. Javey *et al*. utilized 8-nm-thick high-*k* ZrO_2 (*k*~25) as the gate insulator to fabricate the CNTFETs. In the experiment, an individual SWCNT prepared by CVD method was connected between two 3-μm-

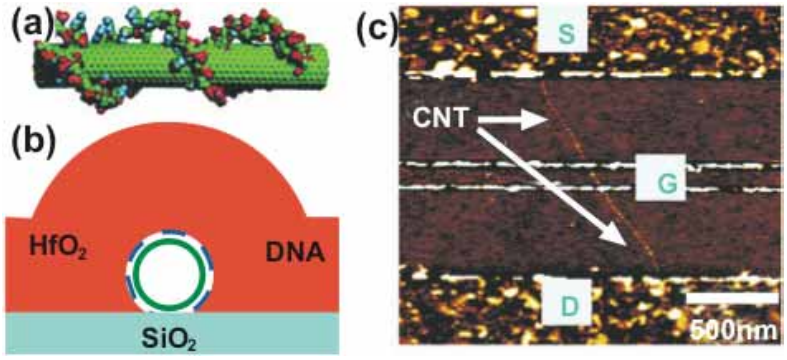

Fig. (5). The CNTFETs fabricated by depositing the HfO_2 on DNA-functionalized SWCNTs with atomic layer deposition (ALD) technique. (**a**) Schematic of a DNA coated SWNT. (**b**) Cross-sectional view of HfO_2 (~3 nm by ALD) conformally deposited on a DNA functionalized nanotube lying on a SiO_2 substrate. (**c**) Atomic force microscopy (AFM) image of a high *k* SWNT FET with top-gate (G) underlapping source (S) and drain (D). Images adapted from reference [20].

gap Mo source and drain electrodes, which were patterned on Si substrate thermally coated by 500-nm-thick SiO_2 layer. And then the thin ZrO_2 was deposited on the SWCNT with the atom layer deposition (ALD) technology. Finally, the 2-μm-width Ti/Au top electrode was fabricated on the ZrO_2 gate insulator. The fabricated CNTFETs exhibited the high device performances: For the p-type CNTFETs, the inverse subthreshold slope of S~70mV/dec was obtained, which approximated the theory limitation (~60 mV) of field-effect transistors under room temperature; the transconductance was 12μS for individual nanotube transistors (3000S/m normalized by double nanotube diameter); The carrier mobility of the devices reached 3000 $cm^2V^{-1}s^{-1}$, which is more than 8 times of p-type Si bulk mobility (450 $cm^2V^{-1}s^{-1}$). For n-type CNTFETs, an inverse subthreshold slope of S~90mV/dec was achieved. The gain of the constructed CMOS with this CNTFETs reached 60, which is highest value reported so far.

On this basis, A. Javey *et al*. integrated the Ohmic contacts and high-*k* gate dielectric technology into the fabrication of CNTFETs to further improve the device performance [22]. In the device, the 8-nm-thick high-*k* HfO_2 (*k*~20) dielectric layer was used as the top-gate insulator which was deposited by ALD technique and Pd metal was adopted to contact the semiconducting SWCNTs. Fig. (**6**) shows the schematic diagram of this CNTFET. In this structure of CNTFETs, the heavily doped Si substrate served as back gate to electrostatically dope the SWCNT. The two ends of doped SWCNT acted as the source and drain electrodes and the SWCNT segment under the top gate served as the conduction channel. The fabricated device exhibited a transconductance of g_m~20μS (5000S/m normalized by double nanotube diameter), an On-state saturation current of I_{ON_sat}~15 μA (~3750μA/μm), and an On-state linear conductance of G_{ON}~$0.1\times4e^2/h$. A rough estimation shows that under the similar gate tuning this g_m and I_{ON_sat} are 5 times higher than that of Si p- MOSFET and 3 times higher than that of the same structure of CNTFET with Mo as contact metal. An inverse subthreshold slope of S~80mV/dec and a current ratio of $I_{ON}/I_{MIN}>10^4$ was achieved by the device. Moreover, the bipolar behavior was also effectively restricted in this CNTFET.

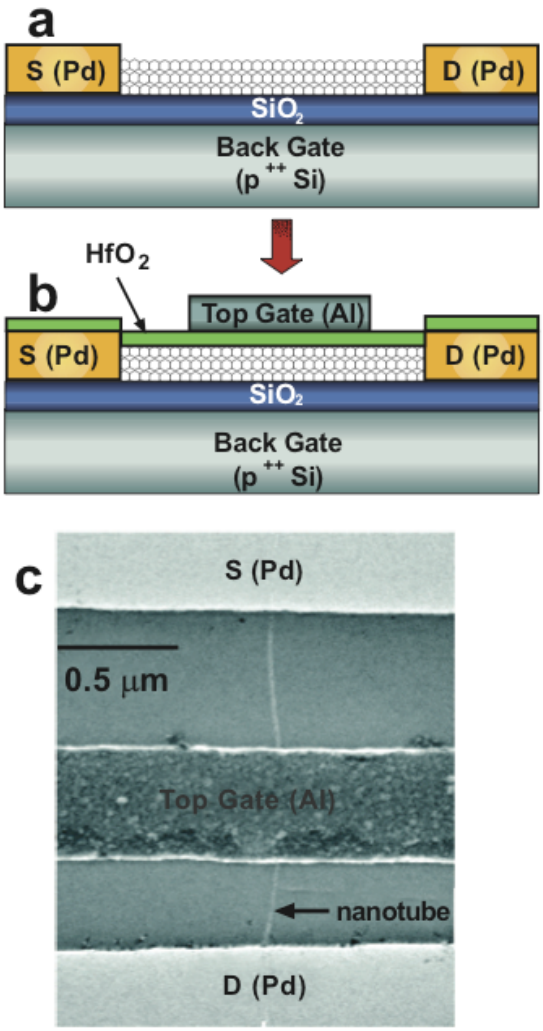

Fig. (6). The CNTFET fabricated by integrating the Ohmic contact and high-*k* gate insulator. (**a**) Schematic device drawings for a nanotube contacted by metal Pd. (**b**) Nanotube FET with HfO_2 fabricated by atomic layer deposition (ALD) as top gate insulator. (**c**) Scanning electron microscopy (SEM) image of the device depicted in **b**. Images adapted from reference [22].

Shorten the SWCNT Channel Length

Another way to enhance the CNTFET performance is shortening the SWCNT channel length. When the SWCNT channel is long (more than several micrometers), the carriers will be scattered in the transport process, which makes the carrier mobility reduced. [23,24] Previous studies had shown that the free path of carriers for the SWCNT could be up to about 500 nm. Therefore, if CNT channel is decreased to a length shorter than this value, the carriers will conduct a ballistic transport in the SWCNT. Thus, the mobility of the device will be greatly increased and the CNTFET fabricated will be effectively enhanced. For this reason, many short channel CNTFETs had been fabricated and researched. R.V. Seidel *et al*. reported a CNTFET with an 18-nm-length channel [25]. They used HSQ (hydrogensilsesquioxane) as the mask to successfully fabricate the very small channel gap (a few more than ten nanometers). Under a drain bias of 0.4 V, the fabricated CNTFET exhibited an On-state current of > 15 μA, a transconductance of 6.75μS and a current ratio of $>10^6$.

However, it should be noted that the improvement effect of this method is degraded when the length of SWCNT channels is smaller than the free path of carriers, which is because the carriers transport ballistically in the SWCNTs and the device mobility is determined mainly by the contact property for this time. Previous studies [26, 27] had shown that when the channel length is smaller than ~260 nm, the influence of the lateral scaling on the performance of CNTFETs is little.

Adopt the Optimized Device Structure

The novel device structures are also adopted to enhance the performance of CNTFETs. Y. M. Lin *et al*. [28] designed a double-gate CNTFET. Fig. (**7**) shows the schematic diagram and subthreshold characteristics of this CNTFET. In this CNTFET, the switch and the injected carrier type were controlled by the Al gate and the Si back gate, respectively. For the effect of Si gate was screened by the Al electrode, SWCNT in the B region would be only regulated by the Al gate, which caused an ideal switch behavior. A subthreshold

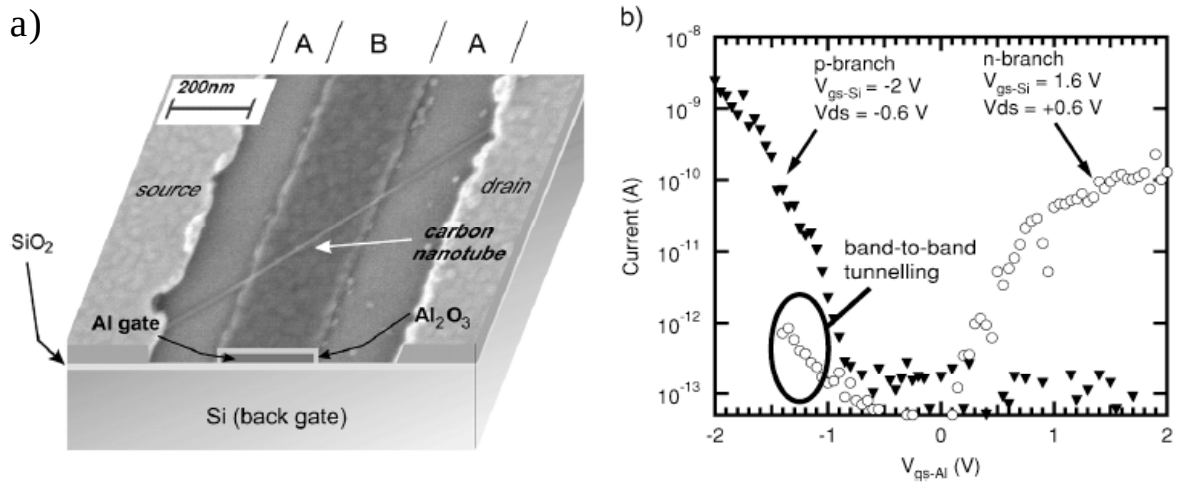

Fig. (7). (**a**) Composite of the device layout of a dual-gate CNFET, showing the SEM image of a CNFET with an Al middle gate underneath the nanotube. (**b**) Subthreshold characteristics (I_d-$V_{gs\text{-}Al}$) of the dual-gate CNFET measured at constant Si gate voltages $V_{gs\text{-}Si}$ =-2 V (▼) and+1.6 V (○), exhibiting clear p- and n-type unipolar behaviors, respectively. Images adapted from reference [28].

slope of ~63mV/dec approximating the theory value and a low OFF current of <100fA can be achieved.

Recently, a novel multi-channel CNTFET has been developed by our research group, in which an array of parallel SWCNTs were nanowelded onto metal electrodes to act as the channels of CNTFETs (see Fig. **8**) [17]. Due to the well-designed device structure and the significantly decreased contact resistance by the ultrasonic nanowelding technique, transconductance and carrier mobility reached 50.2 μS and 7160 $cm^2 V^{-1} s^{-1}$ for p- multi-channel CNTFETs, and 36.5 μS and 5311 $cm^2 V^{-1} s^{-1}$ for n- multi-channel CNTFETs, respectively. The comparison of key device parameters for the fabricated multi-channel and single-channel CNTFETs (see Table **1**) shows the superiority of this multi-channel CNTFETs. A high gain of up to 31.2 had been achieved by the complementary inverters constructed with the p- and n-multi-channel CNTFETs. Besides, this multi-channel CNTFET was also demonstrated to hold better reliability and applicability than the single-channel CNTFETs [29, 30].

Especially, a coaxial surrounding-gate CNTFET (see Fig. **9a**) is predicted to have the excellent device performance, in which the CNT is enwrapped by a thin insulator layer with an equivalent thickness of ~ 1 nm. The device performance is greatly enhanced because of the efficient gate tuning effect for this CNTFET. This coaxial surrounding-gate CNTFET will be hopeful to be used to construct the vertical integrated structure (see Fig. **9b**) [31]. Compared to the state-of-the-art best ballistic double-gate Si-MOSFET, this vertical CNTFET shows the superior device performance (Fig. **9c**), which is enough to meet the requirement of the ITRS road-map in 2016 for traditional Si-MOSFETs [32].

CONCLUSIONS AND PROSPECT

The important optimization methods of CNTFETs have been summarized and reviewed in this paper. With these optimization methods, a great research progress for CNTFETs has been gained. Though some difficulties such as the separation of semiconducting and metallic CNTs still need to be broken through before the industrial application of CNTFETs, the experimental and theoretic study results have shown its bright prospect. With the continual down-scaling of silicon CMOS transistors, the CNTFETs will take over traditional silicon transistors ultimately when the problems resulting from increasing power dissipation, leakage

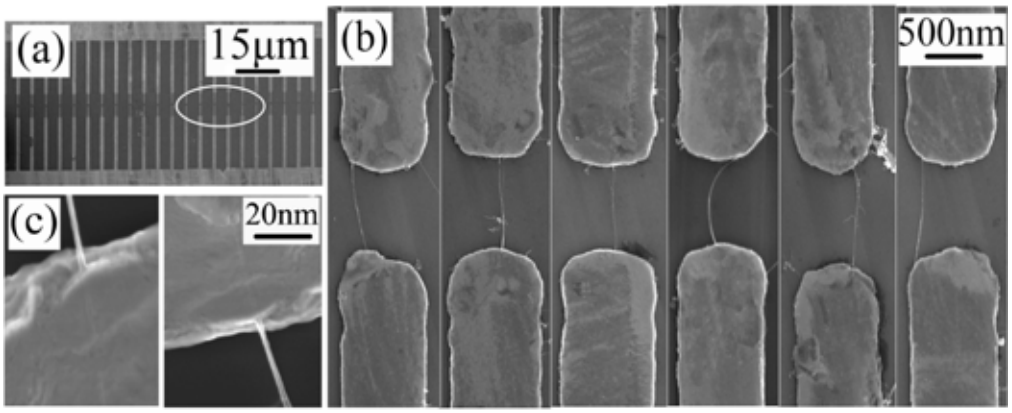

Fig. (8). (**a**) Low-magnification SEM image of an electrode array with 22 diametrically opposed finger pairs. (**b**) Zoom-in view of a local region at the electrode gap, showing that each finger pair is bridged by one SWCNT. (**c**) SEM images of the SWCNT ends nanowelded onto the metal electrodes. Images adapted from reference [17].

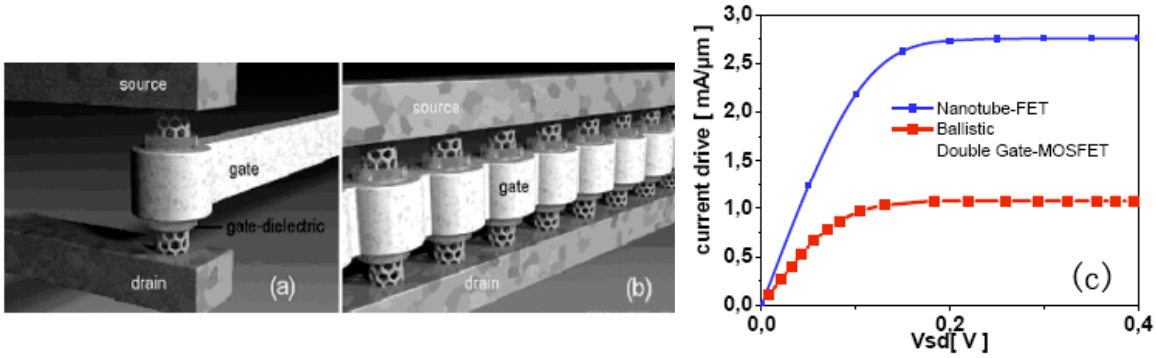

Fig. (9). (**a**) Vertical CNTFET concept; (**b**) Parallel operation of many VCNTFETs; (**c**) show output characteristic of VCNTFET is superior to the ballistic double gate Si-MOSFET. Images adapted from reference [31,32].

currents, and variations in device parameters etc. become insurmountable [8].

Table 1. Key Device Parameters of the MC- and SC-CNTFETs

	Non-Nanowelded Au-Contacted SC-CNTFET	Nanowelded Au-Contacted MC-CNTFET	Nanowelded Al-Contacted MC-CNTFET
Channel length (μm)	1	1	1
Channel number	1	15	13
Drain bias (V)	-0.15	-0.15	0.15
I_{ON} (μA)	0.014	235	196
g_m (μS)	0.028	50.2	36.5
R_{ON} (KΩ)	10 714	0.64	0.77
mobility* ($cm^2 V^{-1} s^{-1}$)	64	7 160	5 311
I_{ON}/I_{OFF}	10^5	10^5 - 10^6	10^6 -10^7
S (mV/dec)	529	116	92
Threshold voltage (V)	-2.5	-0.55	0.65

*The field-effect mobility μ is derived at the drain bias of V_{DS}=±10mV. A gate-channel capacitor of ~0.502 fF and ~0.436 fF is deduced respectively for the p- MC-CNTFET with 15 channels and n- MC-CNTFET with 13 channels.
Table adapted from reference [17].

REFERENCES

[1] Bathtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science*, **2001**, *294*, 1317.

[2] Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom M.; Dai, H. *Nat. Mat.*, **2002**, *1*, 241.

[3] Derycke, V.; Martel, R.; Appenzeller, J.; Avouris, Ph. *Nano Lett.*, **2001**, *1*, 453.

[4] Lin, Y. M.; Appenzeller, J.; Knoch, J.; Avouris, Ph. *IEEE Trans. Nanotechnol.*, **2005**, *4*, 481.

[5] Hur, S. H.; Yoon, M. H.; Gaur, A.; Shim, M.; Facchetti, A.; Marks, T. J.; Rogers, J. A. *J. Am. Chem. Soc.*, **2005**, *127*, 13808.

[6] Oh, H.; Kim, J.J.; Song, W.; Moon, S.; Kim, N.; Kim, J.; Park, N. *Appl. Phys. Lett.*, **2006**, *88*,103 503.

[7] Yang, M. H.; Teo, K. B. K.; Gangloff, L.; Milne, W. I.; Hasko, D. G..; Robert, Y.; Legagneux, P. *Appl. Phys. Lett.,* **2006**, *88*, 113 507.

[8] Avouris, P. Supertubes. *In IEEE Spectrum*, **2004**, *41*, 40.

[9] Tans, S. J.; Verschueren, A. R. M.; Dekker, C. *Nature*, **1998**,*393*, 49.

[10] Martel, R.; Wong, H. S. P.; Chan, K.; Avouris, P. *in IEDM Tech. Dig.*, **2001**, 159.

[11] Zhou, C. W.; Kong, J.; Dai, H. *Appl. Phys. Lett.*, **2000**, 76,1597.

[12] Nihey, F.; Hongo, H.; Ochiai, Y.; Yudasaka, M.; Iijima, S. *Jpn. J. Appl. Phys.*, **2003**, *42*, L1288.

[13] Javey, A.; Guo, J.; Farmer, D.B.; Wang, Q.; Wang, D.; Gordon, R.G., Lundstrom, M.; Dai, H. *Nano Lett.*, **2004**, *4*, 447.

[14] Javey, A.; Tu, R.; Farmer, D. B.; Guo, J.; Dai, H. *Nano Lett.*, **2005**, *5*,345.

[15] Chen, C. X.; Yan, L. J.; Kong, E. S. W.; Zhang Y. F. *Nanotechnol.*, **2006**,*17*,2192.

[16] Chen, C. X., Liu, L.Y.; Lu, Y.; Sheng, X.J.; Ding, H.; Zhang, Y. F. *Carbon*, **2007**,*45*,436.

[17] Chen, C. X.; Xu, D.; Kong, E. S. W.; Zhang, Y. F. *IEEE Electron Device Letters*, **2006**, *27*,852.

[18] Wind, S. J.; Appenzeller, J.; Martel, R.; Derycke, V.; Avouris, P. *Appl. Phys. Lett.*,**2002**, *80*, 3817.

[19] Bathtold, A.; Hadley, P.; Nakanishi, T.; C. Dekker. *Science*, **2001**, *294*, 1317.

[20] Lu, Y.R.; Bangsaruntip, S.; Wang, X.; Zhang, L.; Nishi, Y.; Dai, H. *J. Am. Chem. Soc.*, **2006**, *128*, 3518.

[21] Appenzeller, J.; Martel, R.; Derycke, V. ; Radosavjevic, M.; Wind, S.; Neumayer, D.; Avouris, P. *Micro. Eng.,* **2002**, *64*, 391.

[22] Javey, A.; Guo, J.; Farmer, D.B.; Wang, Q.; Wang, D.; Gordon, R.G.; Lundstrom, M.; Dai, H.J. *Nano Lett.*, **2004**, *4*, 447.

[23] Appenzeller, J.; Knoch, J.; Radosavljevic, M.; Avouris, P. *Phy. Rev. Lett.*, **2004**, *92*, 226802.

[24] Fuhrer, M. S.; Kim, B. M.; Durkop, T.; Brintlinger, T. *Nano Lett.*, **2002**, *2*, 755.

[25] Seidel, R. V.; Graham, A. P.; Kretz, J. R. B.; Rajasekharan, B.; Duesberg, G. S.; Liebau, M.; Unger, E.; Kreupl, F.; Hoenlein, W. *Nano Lett.*, **2005**, *5*, 147.

[26] Wind, S. J.; Appenzeller, J.; Avouris, P. *Phys. Rev. Lett.*, **2003**, *91*, 058301.

[27] Wind, S. J.; Radosavljevic, M.; Appenzeller, J.; Avouris, P. *J. Vac. Sci. Technol. B*, **2003**, *21*, 2856.

[28] Lin, Y. M. ; Appenzeller, J. ; Knoch, J. ; Chen, Z.; Avouris, P. *IEEE Transactions on Nanotechnology*, **2005**, *4*, 481.

[29] Chen, C. X.; Zhang, Y. F. *J. Nanosci. Nanotechnol.*, **2006**, *6*, 3789.

[30] Chen, C.X.; Liu, L.Y; Liu, X.; Kong, E. S. W.; Miao, J. P.; Zhang, Y. F. *Phys. Lett. A*, **2007**, *366*, 474.

[31] Hoenlein, W.; Kreupl, F.; Duesberg, G. S.; Graham, A.P.; Liebau, M.; Seidel, R.V.; Unger, E. *IEEE Trans. Comp. Packaging Techn.*, **2004**, *27*, 629.

[32] Guo J, Lundstrom M, Datta S. *Appl. Phys. Lett.*, **2002**, *80*, 3192.

Received: June 4, 2007 Revised: July 13, 2007 Accepted: July 20, 2007