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III-V Compounds-on-Si: Heterostructure Fabrication, Application and Prospects

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Abstract: While silicon and gallium arsenide are dominant materials in modern micro- and nanoelectronics, devices fabricated from them still use Si and GaAs substrates only separately. Integrating these materials on the large and cheep Si substrate has been the subject of enormous research efforts for the past three decades. This review attempts to systematize and generalize the current understanding of the fundamental physical mechanisms governing the epitaxial growth of GaAs and related III-V compounds on Si substrates. Different kinds of bonding as a very promising non-epitaxial method for III-V thin film integration on Si substrate are reviewed. Basic techniques available for improving the quality of such heterostructures are described, and recent advances in fabricating of device-quality III-V-on-Si heterostructures and corresponding devices are also presented.

1. INTRODUCTION

Silicon is and will be the basic material for solid-state electronics. About 95% of all semiconductor devices are presently fabricated using silicon wafers. As a carrier, a Si wafer is undoubtedly advantageous due to its light weight, higher thermal conductivity, low cost, up to 300 mm substrate diameter and very mature technology. On the other hand, III-V compounds (and first of all, GaAs), following Si in the known list of most important semiconductor materials, are the major ingredients for optoelectronics and, due mainly to a considerably higher electron mobility, they are very suitable for very fast operation devices. It is only natural therefore that researchers all over the world wanted to combine these materials on a Si wafer for quite some time.

The first step on the way in this trend is obtaining high-quality thin GaAs layers on Si wafers, the so-called artificial or alternative wafer platforms. Such GaAs-on-Si wafers are supposed to have a considerable market potential both for the replacement of an expensive GaAs wafer in fabrication of traditional devices (microwave devices, solar cells, photodetectors) and for monolithic integration of high-performance GaAs devices with high-density silicon integration circuits. The wish to realise these aims was a driving force for numerous investigations in both epitaxial growth of III-V compounds on Si wafers and elaboration of wafer bonding techniques of these compounds to Si.

2. III-V-ON-SI BY EPITAXY

2.1. Direct GaAs-on-Si Epitaxy

The first successful experiments in GaAs growth on Si wafers date back to the 80's of the last century (see e.g. [1-5]). Historically, the first experiments in GaAs growth on Si wafers have been conducted by means of growing this material directly on Si [1-13]. By the onset of the last decade of the XXth century the basic problems were found out and laid down in the wide review by Fang *et al.* [14]. It is, first of all, the growth of polar semiconductor on a non-polar semiconductor leading to high density antiphase domains formation. The pure (001) silicon surface consists of, mainly, monoatomic steps on the surface of which Si atoms are arranged as dimers directed perpendicularly to each other on the neighbouring terraces. Passivation of such a surface with arsenic, i.e. covering Si surface with As monolayer — at the initial stage necessary for polar compound growth on the non-polar wafer — leads to the formation of As dimers directed also perpendicularly to each other on the neighbouring terraces. GaAs nucleus appeared on the neighbouring terraces will also be turned to each other at 90^0 round the vertical axis. Imperfections of crystal structure turn up during their growth and coalescence, and they are called antiphase defects. This problem was successfully resolved using Si wafers misoriented from the singular plane (001) by 4-6 arc degrees (see e.g. [7]). On such a Si wafer surface two-atomic steps develop, and Si-Si dimers have the same orientation forming the so-called single domain surface. As a consequence, in the As monolayer deposited onto Si surface before GaAs growth onset, arsenic dimers also have identical orientation and, after applying Ga, GaAs crystallites of one sign are formed.

Other problems turned out more serious. Dislocation density in GaAs film reaches the values of 10^9-10^{10}cm^{-2} due to the difference between the film and wafer lattice parameters close to 4% in the system of GaAs/Si. The difference in thermal expansion coefficients (6.63×10^{-6}K^{-1} and 2.3×10^{-6}K^{-1} for GaAs and Si, respectively) also promotes the formation of a big number of dislocations and appearing of cracks in the GaAs film during cooling. These problems are still a serious obstacle for epitaxial growth of high quality GaAs films less than one micron thick on Si wafers.

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The mechanism of new phase formation via islands (three-dimension, 3D growth) is one of the fundamental reasons for a big number of defects in GaAs/Si films at the initial stage of epitaxial growth. According to Asai *et al*. [15], the reflection high-energy electron diffraction (RHEED) turned to spotty that corresponds to the growth onset by the island mechanism — already after applying GaAs film onto Si, average thickness being 1 monolayer, and even more obvious when it is 2 monolayers thick. Typical picture of RHEED spotty patterns just at the initial part of GaAs growth is presented in Fig. (**1**). We can see the spotty patterns which are connected by tension bars reflecting the facet sides appearing. Investigation of such a surface using atomic-force microscopy (AFM) is indicative of the appearance of islands having density of $10^{11}cm^{-2}$. GaAs/Si islands have the ratio of height to the lateral size being close to ½ at the initial growth stage [16, 17]. Later on, as an average GaAs layer thickness increases, the islands shape changes slightly, and it can be observed in the papers by Fang *et al*. [14] and Tsai *et al*. [16] on transmission electron microscopy (TEM) images of cross-sections of such structures and also on AFM images [17, 18]. Recently Usui *et al*. [17] have shown that hemispherical and dislocated GaAs islands are grown on the Si substrate as early as only 4 GaAs monolayers at 400 ^{0}C are supplied.

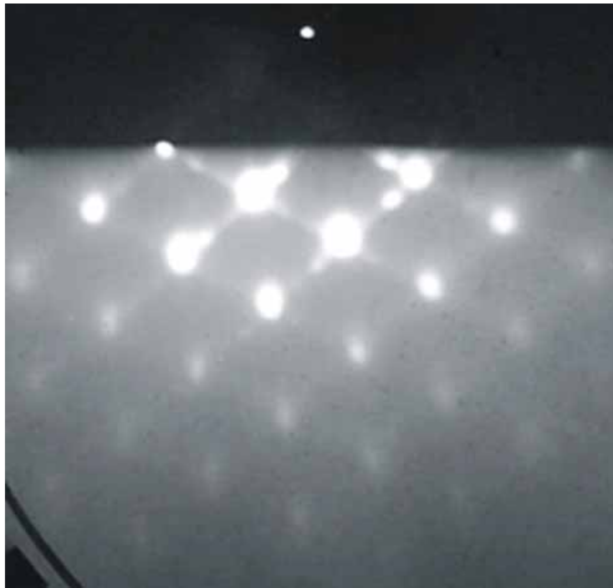

Fig. (1). RHEED patterns of GaAs/Si epitaxial growth at the initial stage: GaAs average thickness is about 1 ML. (This picture has been provided by M. A. Putuato).

Different methods and techniques that allow us to decrease the dislocation density at the by-surface GaAs layer region down to ~10^6cm^{-2} have been worked out for thicker GaAs/Si layers. It is, first of all, thermal cycle annealing (TCA) [10, 11, 13] and also using lower temperatures at the initial part of GaAs growth— the so-called two-step growth [6, 18-25]. The first step is either some nanometers (or tens of nanometers) of GaAs grown at low temperatures or molecular enhanced epitaxy (MEE) by alternating Ga and As. Solid-phase crystallisation of amorphous GaAs layer can also be referred to the first step. The basic part of GaAs layer is then grown under the conditions standard for this material. Insertions in GaAs layer volume as ultra-thin epitaxial layers of Si, InGaAs strained material and also strained superlattices [8, 12, 26] actively initiate annihilation of threading dislocations (TD).

The general structural quality of GaAs films grown on Si (001) can be estimated with X-ray rocking curves from the film in planes (004) reflection. Full width on a half maximum (FWHM) directly depends on defects concentration in the film. Measured by different authors, FWHM values on GaAs films of various thicknesses grown directly on the Si wafer having orientation (001) are shown in Fig. (**2**). These dots array is pointed out as a shaded area. A big diversity of half-width values for the same GaAs film thicknesses is observed. Dashed downward arrows show a considerable improvement of film structural characteristics for one and the same thickness when using TCA [19, 27-32]. Intermediate layer insertions with another lattice parameter also contributed to FWHM decrease (insertion Si [29], insertion InGaAs [31]). Li *et al*. grew GaAs epilayers on a SiO_2-patterned silicon substrate [33]. They have shown that dislocations in such heterostructures can be largely eliminated by trapping on vertical dielectric sidewalls. As one can see in Fig. (***2a***) the value of FWHM taken from this work is finding in the bottom part of the shaded area.

The theoretical dependence (dashed line) of FWHM on perfect (dislocation-less) film thickness whose value decreases only by an increasing number of the perfect crystal reflecting planes is also depicted in Fig. (**2**). GaAs epitaxial films being grown on Si wafer can not get closer to this dependence in their structural perfection as their pseudomorphic and, respectively, defect-less state is possible only at the stage of separate nucleus. After the beginning of GaAs film plastic relaxation with the formation of a big number of defects at the interface, FWHM can not be close to the theoretical dependence — as is seen in Fig. (**2**). Fig. (***2b***) is a simplified version of Fig. (***2a***) that allows us to compare GaAs/Si experimental results to FWHM values for the films obtained in another way. If we assign only the best results from papers in which GaAs films grown directly on Si were investigated these results hit in the hatched oval in Fig. (***2b***).

There are some other ways of putting GaAs on Si. Thus, the FWHM value for GaAs film being 2.5 µm grown on the Si wafer over the buffer Ge/GeSi taken from Luo *et al*. [34] is shown in Fig. (**2**). This value, equal to 120 arc sec. is currently the lowest for the corresponding GaAs film thickness epitaxially grown on the Si wafer. In this GaAs/Ge/GeSi/Si heterostructure the basic dislocation array, responsible for the compensation of lattice parameter misfit for GaAs and Si, is located inside the buffer GeSi layer and it only slightly affects the widening of X-ray rocking curves for the GaAs film. Tanoto *et al*. [35] grew GaAs on Ge/Si platform using MEE method on the initial part of the growth. Then, a standard GaAs MBE growth process was used to grow a structure comprising a 250-nm thick GaAs, 6-nm-thick $In_{0.2}Ga_{0.8}As$ single quantum well, and a 100-nm-thick GaAs cap layer. As authors have reported the FWHM of the layer peak of the GaAs film about 0.35 µm thick with inserted InGaAs thin layer was 160 arc sec. As can be seen in Fig.

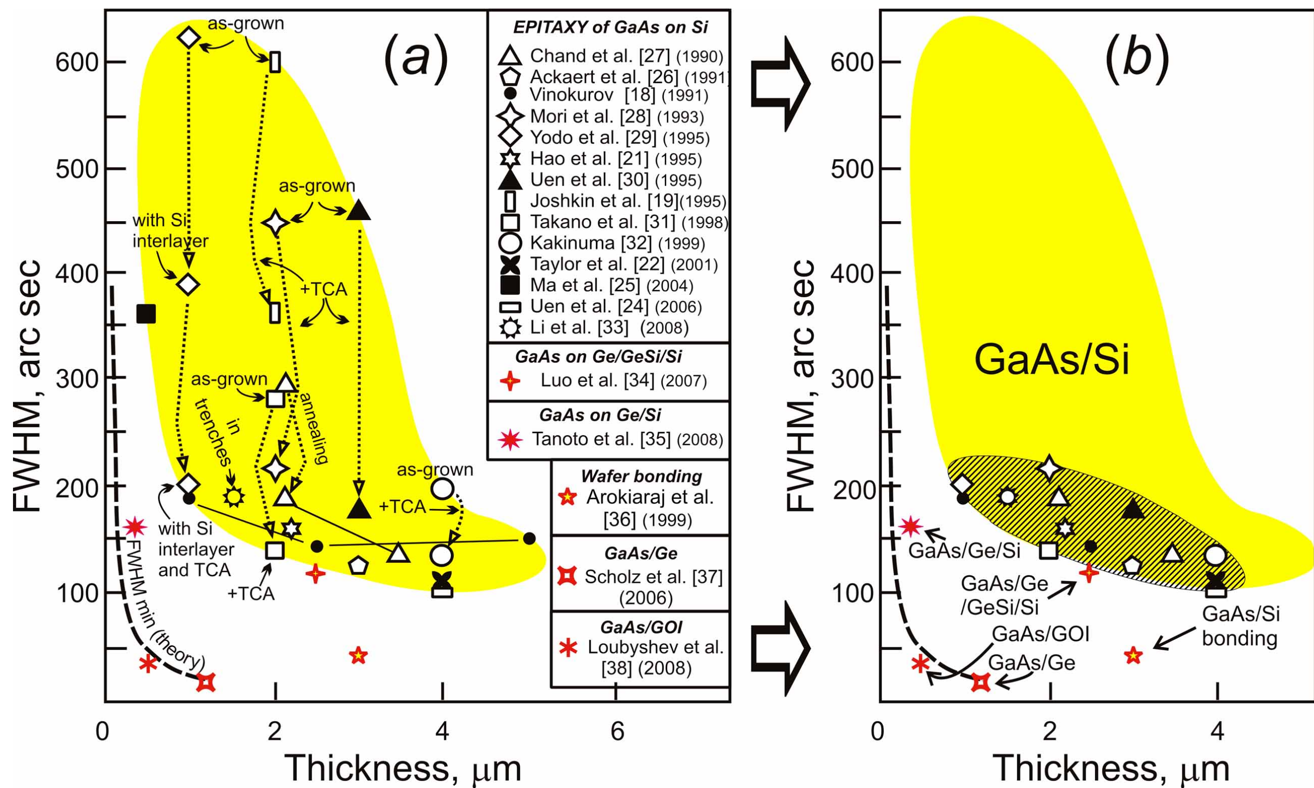

Fig. (2). Full width at a half-maximum of the (004) GaAs X-ray peak (FWHM) according to different authors in depending on GaAs film thickness. Dashed line is the theoretical curve for pseudomorphic defect-less film. (**a**) - experimental dot array for GaAs films, grown directly on Si, is inside of the shaded area. Intermediate experimental dots of this array and also references are omitted in (**b**) for easier perception and comparison with other data. Only the best results from papers in which GaAs films grown directly on Si were investigated are preserved in the hatched oval in Fig. (**2*b***). Red points (color on line) are for the GaAs films whose direct growth on Si was avoided.

(**2**), such value of FWHM is also minimal in comparison with FWHMs for GaAs films directly grown on Si.

There are non-epitaxial methods of thin GaAs film organisation on the Si wafer- the so-called wafer bonding technique. According to this technology, the GaAs film grown on the GaAs wafer is separated from this wafer and transferred to the Si wafer (the corresponding methods are considered in more detail in Chapter 3). In this case there are no defects inevitably appearing in the film under heteroepitaxy, and the FWHM value is determined by imperfections occurring during homoepitaxial GaAs/GaAs growth and bonding to the Si wafer. Thus, Arokiaraj *et al*. [36], having realised the bonding of GaAs film to the Si wafer and having removed the GaAs wafer using selective etching, note that the FWHM of such a 3μm GaAs film is equal to 44 arc sec. (Fig. **2**). This value is minimal for all GaAs/Si films some microns thick. The best results in FWHM of GaAs films are observed when they are grown on the Ge or GOI wafers (Ge-on-Insulator, - Ge on Si by bonding, for more details on such platform see Chapter 3). Thus, the FWHM values of GaAs/Ge and GaAs/GOI borrowed from Scholtz *et al*. [37] and Loubyshev *et al*. [38] are hit on or near of the theoretical dependence (Fig. **2**).

Therefore, comparison of FWHM values for GaAs films grown directly on Si wafers (hatched oval in Fig. **2*b***) to the results obtained on GaAs/Ge(GeSi)/Si platforms and, especially on GaAs/Ge, GaAs/GOI and GaAs-on-Si by bonding are in favour of the methods in which the difference in lattice parameters between GaAs film and the wafer is either practically absent or was overcome by wafer bonding.

2.2. GaAs-on-Si Growth Through Buffer Layers

As is seen in Fig. (**2**), the least FWHM value for the GaAs films of a certain thickness epitaxially deposited on Si is observed under the buffer Ge or Ge/GeSi layer introduction between the film and the wafer. The method of fabricating of Ge/GeSi/Si-related artificial wafer - where GeSi is an intermediary layer with a changing lattice parameter that ends in pure Ge, - is the most developed. GaAs and Ge have close values of lattice parameters and thermal expansion coefficients. Earlier investigations in growing perfect GaAs films on Ge wafers showed that antistructural defects and antiphase borders [39, 40] were the basic imperfections, and their density was reduced to zero by a certain wafer deviation at some degrees from (001) orientation [41, 42]. As can be seen in Fig. (**2**), the FWHM value for GaAs onto Ge is close to the theoretical one. Therefore, it was logical to implement GaAs growth on Si wafers through buffer layers having pure Ge on their surface.

The founding research in fabrication of GeSi buffer on Si layers was published in 1991, Fitzgerald *et al*. [43]. It was reported on Ge_xSi_{1-x}/Si(001) film growth (x equal to ~0.5) with TD density not more than 2×10^6cm^{-2}. The following problems were revealed at already this stage: to fabricate GeSi films with the above-mentioned density, the gradient of Ge composition must not to exceed 10% of Ge per micron of

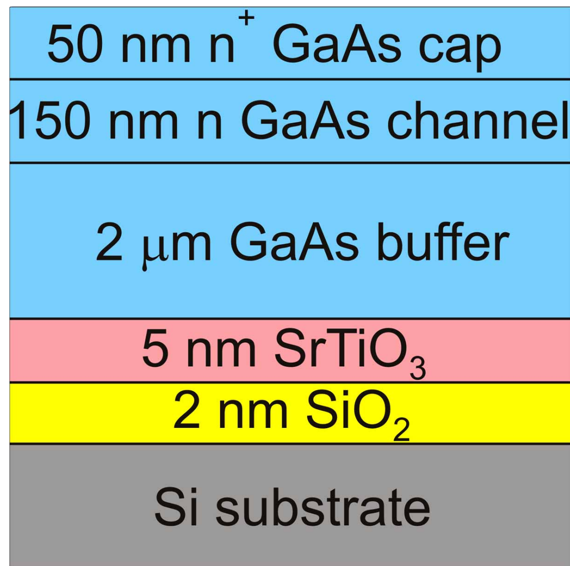

Fig. (3). Scheme of GaAs/STO/Si heterostructure according to Eisenbeiser *et al*. [64].

buffer layer thickness. It led to a big material consumption and the necessity for high growth temperatures (~ 900 ^{0}C) to ensure the acceptable heterostructure growth cycle time. High growth temperature, in its turn, contributed to a considerable increase of roughness of the final product surface that reached hundreds of nanometers [44]. The problem of surface roughness was partially resolved using Si wafers misorinted a few degrees from exact orientation (001) and chemical polishing of film surface [45]. Simultaneously, the composition of buffer Ge_xSi_{1-x} layer was achieved being equal to x = 1, i.e. the aim of film growth with a 100% Ge content was achieved. Having applied chemical polishing of Ge_xSi_{1-x}/Si(001) heterostructure at the intermediary growth stage, x = 0.5, with further GeSi buffer layer on-growth till pure Ge, the authors [46] demonstrated the possibility of fabricating artificial Ge/GeSi/Si(001) wafers with TD density in top Ge layer not more than 2×10^6cm^{-2}. The basic achievements of this method in fabrication of field effect transistors (FETs) with strained Si, GeSi and Ge channels were published in review of Lee *et al.* [47]. GaAs film growth on Ge/GeSi/Si(001) platform and investigation of their properties became a natural expansion of using such a platform [48].

To date dislocation density in the functional part of epitaxial GaAs film can be decreased down to 10^6cm^{-2} only using gradient buffer GeSi layers. Respectively, the life time of minority carriers in GaAs (heterostructures of AlGaAs/GaAs/AlGaAs type grown on platform Ge/GeSi/Si) reached the value exceeding 10 ns [49]. Such high structural parameters of GaAs/Ge/GeSi/Si platform enabled to fabricate a number of devices working on the minority carriers: solar cells, LEDs and injection lasers. By the present, all the basic device types earlier implemented in GaAs/GaAs and GaAs/Ge heterostructures have also been fabricated with GaAs/GeSi/Si: solar cells [49-53], LEDs and lasers [54-58] (including also laser-PIN diode-like optical connections [59]), transistors [60]. The major contribution to this trend belongs to a group of Massachusetts Technological Institute headed by Fitzgerald [49-52, 54, 55, 57-60].

It is worth focusing on one more possibility of growth — that of growing GaAs/Si through the intermediate $SrTiO_3$ (STO) layer. Such a way of growing GaAs was first announced in 2001 [61]. The earlier worked out methods for epitaxial deposition of STO insulator onto Si [62] was used for GaAs epitaxial growth over this insulator [63, 64]. STO growth was initiated with combined Sr and Ti deposition at oxygen ambient atmosphere at wafer temperature in the range of 200-400 °C [62, 65]. The GaAs/$SrTiO_3$/Si heterostructure is schematically presented in Fig. (**3**). The SiO_2 layer located between STO and Si is supposed to form after STO growth as a result of oxygen diffusion in Si at a certain temperature and can be used as an insulator separating the epitaxial structure from the wafer. It was reported on high qualities of grown heterostructures: dislocation density in GaAs was about 10^5cm^{-2}, surface roughness mean-square value was about 0.9 nm, antiphase domains were absent. Electron mobility in GaAs/$SrTiO_3$/Si was 94% from that of control GaAs/GaAs sample [64].

It was reported in [63] that GaAs/STO/Si heterostructures of device quality were grown on Si wafers 200 and 300 mm in diameter with molecular beam epitaxy (MBE) method at "Motorola Inc." laboratories. FETs fabricated on such heterostructure showed optimistic results: after 800 hours of operation at 200 °C the channel current degradation was 1.2% in sample GaAs/STO/Si. Chediak *et al*. [66], analysing these experiments, came to the conclusion that the authors of [63, 64] could successfully fabricate the device quality GaAs-on-Si films. However, the mechanisms responsible for the perfect GaAs film growth in GaAs/STO/Si configuration were not revealed, and our search over databases did not found any continuation of this work and parallel investigations in this trend by other researchers.

Dislocations are the basic defects worsening the device parameters on GaAs/Si. The most significant and replicated data on their least density in such epitaxial heterostructures are close to value 10^6cm^{-2}. For transistors operating on majority carriers, a high dislocation density manifests itself in reduced electron (or hole) mobility, whereas minority-carrier devices (solar cells, light diodes, and injection lasers) are more sensitive to these defects. Dislocation density in such structures should be less than 10^6cm^{-2}. As already noted earlier, Motorola-produced FETs based on GaAs/STO/Si heterostructures MBE-grown on Si substrates have very similar properties to reference GaAs/GaAs samples [62-64]. At the same time, lasers made on GaAs/Ge/GeSi/Si-like platform with dislocation density equal to 2×10^6cm^{-2} in GaAs were functional for not more than 4 hours [55].

In [67] it is reported on InGaAs/InAlAs/GaAs/Si heterostructure growth, on which FETs with quantum well $In_{0.7}Ga_{0.3}As$ were fabricated. The buffer layer general thickness was 3.2 μm at 2 μm GaAs. According to the authors, TD density was not tested in the channel area on the structure's cross-section, i.e. it was less than 10^8cm^{-2}. TD density, obviously, considerably decreases in the buffer InAlAs layer. These heterogeneous III–V transistors on silicon substrate show performance characteristics equal to those previously

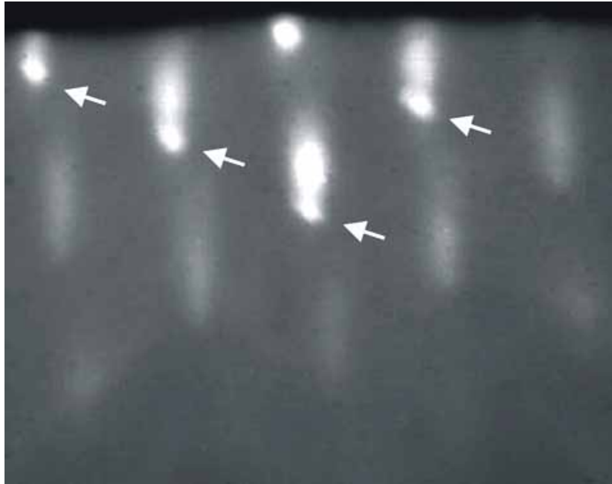

Fig. (4). RHEED patterns for the initial growth of GaP-on-Si. 4 monolayers of GaP are grown by MEE [71].

achieved on pseudomorphic $In_{0.7}Ga_{0.3}As$ HEMTs on InP substrate.

Despite certain successful achievements in device fabrication based on GaAs and other III-V compounds grown on Si wafers, the solution for the problem of integrating GaAs optoelectronics and traditional Si integrated circuits on one substrate by growing GaAs films on Si wafers is still open. A big distance in thickness between GaAs and Si surfaces exceeding 10 μm, when using graded Ge/GeSi buffers on Si wafers, is a serious barrier for using high-resolution lithography methods for connects between Si and III-V neighbours on the wafer. Therefore, researchers are now more focused on non-epitaxial bonding methods for heterogeneous materials that allow making them closer to each other at the distance less than 1 micron without any vivid worsening of their structural perfection.

2.3. GaP-on-Si Epitaxy

2.3.1. Initial Stages

Epitaxial GaP films on Si wafers are used as the first step in the transfer from Si to GaAs [68, 69], and also they are important proper as a basic element for different device applications [70]. A comparatively small difference between GaP and Si (0.37%) lattice parameters is a reliable factor. However, detailed studies of RHEED-assisted GaP-on-Si (001) initial growth stages showed that obtaining a perfectly continuous GaP layer at the initial growth stage is the main problem here (just as in GaAs/Si). Practically all researchers report that RHEED patterns show the formation of spotty reflections that correspond to 3D growth, right after the beginning of GaP-on-Si epitaxial growth. An example of such tendency is presented in Fig. (**4**) where the bright spots in the base of reflexes are seen [71].

The difference between GaP and Si lattice parameters increases with temperature and is already equal to 0.5% at T~400 ^{0}C. Critical film thickness at which introduction of misfit dislocations (MDs) is energetically efficient and plastic relaxation of GaP layer becomes possible does not exceed 20 nm for temperatures 400-500 ^{0}C in accordance to Matthews and Blakeslee [72] model. Thus, when the GaP film thickness exceeds this value and there is a sufficient number of MDs centres, its plastic relaxation will begin. Under ordinary regimes, in which the GaP-on-Si island growth is realised, the faceted film surface (after islands coalescence) is an active source of dislocations.

It is possible to point out some research papers significant for understanding the peculiarities of GaP-on-Si(001) [70, 73-80] growth. Continuous, supposedly pseudomorphic at their initial stage GaP/Si films, could be observed only when grown with metal-organic chemical vapour deposition (MO CVD) method [81, 82]. The following can be referred to the proofs in these papers in favour of GaP films of possible pseudomorphic state: absence of defects in cross-section TEM images of films 90 nm thick observed in work of Soga *et al*. [81]; the additional periodic peaks seen on the GaP film X-ray rocking curves - so called thickness fringes resulted in report of Kunert *et al.* [82]. Presence of hydrogen in the reactor atmosphere under MO CVD growth is, obviously, a factor contributing to GaP/Si film surface planarisation at its initial growth stages.

Takagi *et al*. [79] note that the Si(001) phosphor-stabilised surface is chemically passive and, even at the initial stage of GaP monolayer deposition, there is a tendency to GaP island formation. Nevertheless, as the authors mention, dislocations were introduced in the continuous layer under Ga and P monolayer alternation growth (MEE), and their generation was not found at the stage of separate islands.

2.3.2. General Structural Perfection

The two-step growth [74, 76, 78], TCA [74] and also using MEE methods [73, 79, 83] led to a considerable improvement in characteristics of GaP-on-Si films. Results of different authors in FWHM dependence on GaP film thickness for the GaP/Si are demonstrated in Fig. (**5**). A big range of data within film thickness to 0.5 μm is observed. This fact confirms the key role of the initial stage of film formation. The theoretical dependence of FWHM for perfect GaP films (dashed curve) is presented in the same Fig. (**5**) allowing the crystal perfection of real films to be estimated. The fact of super low values of FWHM in works by Sadeghi and Wang [73] and Yu *et al*. [70] for thicknesses 0.2 and 0.4 μm, respectively, is outstanding. These values are pointed out in dashed oval in Fig. (**5**). For the left point (Sadeghi and Wang [73], film thickness 0.2 μm) one can suppose that this film is close to the pseudomorphic defect-less state and, therefore, FWHM has a small value close to that of theoretical. As a proof for the existence of such films, we used the data from Kunert *et al*. report [82], in which the thinnest GaP-on-Si films ever reported were studied by X-ray diffractometry. It is seen from Fig. (**5**) that these values practically coincide with the theoretical dependence, and it indicates the absence of defects in these films. This fact proves the possibility of growing a continuous defect -free pseudomorphic GaP-on-Si(001) layer. Nevertheless, after the GaP film exceeds some thickness, introduction of MDs becomes inevitable. As is shown in the Fig. (**5**), the FWHM of the thicker (0.5 μm) GaP film from Sadeghi and Wang [73] (experimental dots of these authors are joined with a dotted line in Fig. **5**) consid-

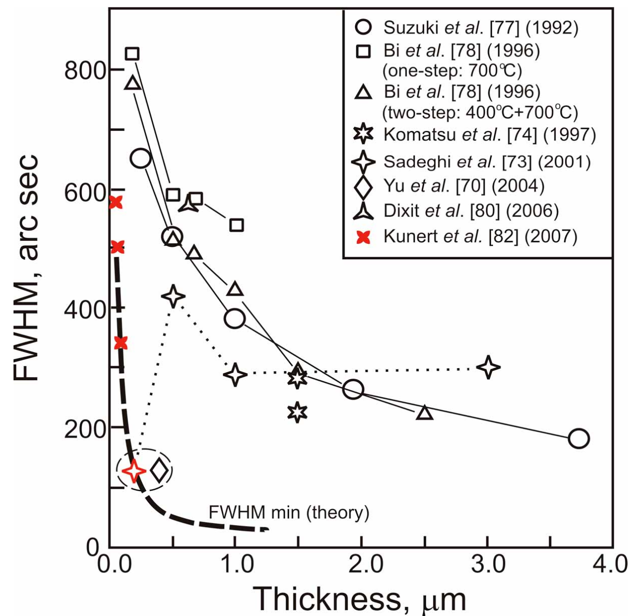

Fig. (5). Full width at a half-maximum of the (004) GaP X-ray peak *versus* the thickness of a GaP film on a Si substrate as presented by various authors. Red points (color on line) hit on the theoretical curve for pseudomorphic defect-less film.

erably increased becoming close to the basic data array for this thickness.

In Fig. (**5**), the right point of the dashed oval (film thickness 0.4 µm), on Yu *et al*. [70] assertion, corresponds to the completely relaxed state. Such a film must inevitably have a certain number of misfit dislocations-like defects and, nevertheless, its FWHM is 130 arc sec. which is the least value published for these GaP/Si thicknesses and that of close to the theoretical one. Explanation of such a difference from the data of other research papers lacks the analysis of such film structural characteristics. However, the appearance up of such parameters should be taken into account.

3. NON-EPITAXIAL III-V-ON-SI TECHNIQUES (BONDING)

The generic term 'wafer bonding' refers to transfer of bulk or thin-film GaAs (as well as other III-V compounds) to various, primarily Si, substrates. Direct bonding of two solid bodies can be carried out even at room temperature by compression of specularly polished plane and totally pure surfaces. The conjoint surfaces interact at the atomic level due to Van der Waals forces. A profound history of such a contact can be found in review of Gösele *et al*. [84]. Thorough processing of conjoint surfaces, including their planarisation, minimisation of roughness value and thorough cleaning to remove any organic and metallic contaminations from the wafer surface [85-87] are necessary for direct bonding of two surfaces. The other bonding type is using high-temperature "sticking" of one solid body to the other by applying glass-like coating on both surfaces being bonded with further compression at the temperature of glass softening. In semiconductor technology, such bonding was first carried out by Antipas and Edgecumbe [88]. Heterostructure GaAs/AlGaAs was bonded to the glass wafer to fabricate a GaAs-based transmission photocathode. GaAs wafer was removed, and thick glass was used as a transparent handle wafer for GaAs/AlGaAs-like device heterostructure.

For the next years, different media for bonding of two heterogeneous materials were elaborated: SiO_2-SiO_2 [89, 90], borophosphorosilicate glass (BPSG) with different forms of coating - to those from liquid phase [91, 92], SeS_2-SeS_2 [36], applying a thin viscous layer on both conjoined substrates with the centrifugal method from solutions based on silane (Si-OH) and methyl (CH_3) polymers solved in alcohol-aceton mixture [93, 94]. The bases of bonding technology for different semiconductor materials can be found in review of Gösele and Tong [95].

The key element in the whole technological chain of bonding a thin film to the handle wafer is working out the methods for donor wafer selective "rejection" or exfoliation following the bonding. One way involves the incorporation of stop layers into the bonding structure. A modern scheme of a GaAs film or a more complicated heterostructure transfer, e.g. laser structure, over to a massive Si wafer is displayed in Fig. (**6**). The transferred heterostructure and Si wafer (Fig. **6*a*** and **6*b***) are coated with an oxide layer and bonded at a certain pressure and oxide softening temperature (Fig. **6*c***). Stop layer in this case is AlGaAs film with a big Al content. It is grown directly on GaAs before the main heterostructure and locks the GaAs wafer etching. GaAs wafer (Fig. **6*d***) and then also the stop layer are etched and, in position of Fig. (**6e**) (dashed oval) we have a new artificial wafer. Then the GaAs layer is either thinned and smoothed by chemical-mechanical polishing till the required thickness and surface smoothness (Fig. **6*f*₁**) or an additional epitaxial growth of a new GaAs layer (Fig. **6*f*₂**) is possible. In all the cases of such artificial GaAs/Si wafer organisation, the donor GaAs wafer is eliminated by etching, and it, naturally, makes such a technology considerably more expensive. Nevertheless, non-epitaxial bonding techniques give us a new degree of freedom allowing creating good quality combinations of materials which could not be realised earlier by single epitaxial growth.

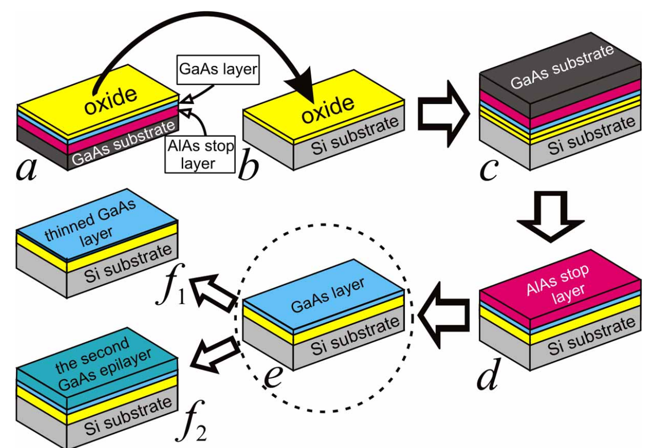

Fig. (6). Schematic of fabricating an artificial GaAs/Si substrate by the wafer bonding method.

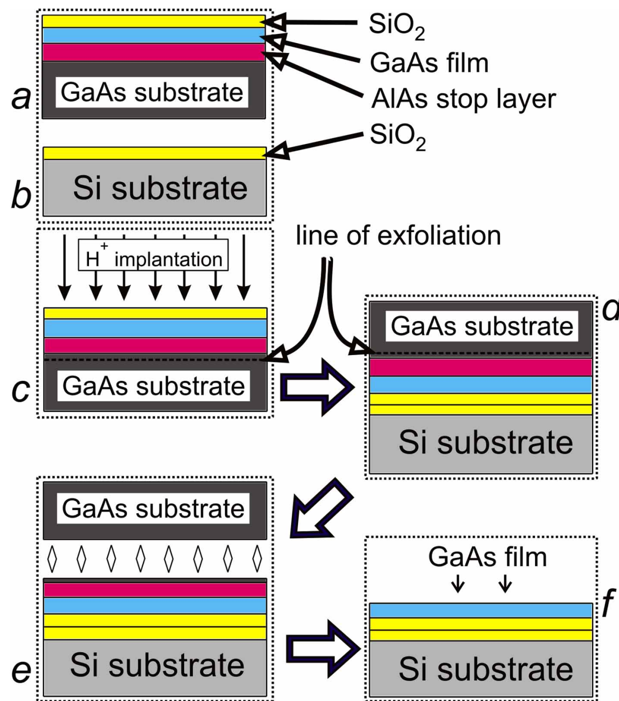

Fig. (7). Detachment (shot-off) scheme for the basic part of donor GaAs wafer using Smart Cut™ technology.

Another way is exfoliation of the main part of GaAs donor wafer based on the Smart Cut™ technology which was worked out earlier for fabrication of SOI (silicon-on-insulator) [96] wafers. The scheme of such exfoliation is presented in Fig. (**7**). Just as earlier (Fig. **6**), the handle and donor wafers are coated with a thin oxide layer, e.g. SiO_2 (Fig. **7*a***, ***b***). Then, a layer of H or He bubbles (Fig. **7*c***) is made in the donor wafer at a certain depth with the ion bombardment method. After wafer bonding (Fig. **7*d***) the exfoliation (Smart Cut™ technology) is realised under heating (Fig. **7*e***). Such exfoliation of the basic part of a donor wafer from that of Si was used for both GaAs and InP [90, 97-99]. After this procedure, the surface of the structure's transferred part is coarse and needs chemical polishing. The stop layer presented in the Fig. (**7**) considerably facilitates the task. III-V-related device heterostructures are grown either on donor GaAs or InP wafers till bonding them to the Si wafer (e.g. laser heterostructures [100-104]) and then, reversed sequence of epitaxial layers is necessary, - or they are grown on the III-V layer left on Si after the bonding and exfoliation of the donor wafer. GaAs or InP wafers are considerably smaller in their diameters compared to those of Si. Therefore, a more perspective way of GaAs-on-Si film fabrication is epitaxial growth of this material on Ge-on-Si platforms. The method of bonding the donor Ge wafer to Si and further exfoliation of Ge layer based on the well-known Smart Cut™ [105, 106] technology is analogous to that described above. In [107] it is reported on the fabrication of GOI platforms on Si wafers of 100-200 mm in diameter, with Ge films being from 200 to 50 nm thick.

Let us point out the advantages of Ge-related wafers over those of GaAs under the growth of III-V-related heterostructures on them: high crystal perfection, higher mechanical strength, big diameters [108]. Earlier, these factors led to a wide use of Ge wafers in growing GaAs/Ge solar cells for telecommunication satellites [109], and they also make Ge a viable competitor for GaAs-related devices different from solar cells. High Ge-on-Si film perfection in GOI-like structures and their electrical isolation from the handle wafer contributed to the intensification of research in the methods of Ge-on-Si structures fabrication and to their diverse device applications (e.g. [110-112]).

GOI wafers are expected to be a promising platform for growing different III-V-based device structures. The work of Thomas *et al*. [113] proves it as an example. According to the authors, they first demonstrate the growth, fabrication and dc device characterization of InGaP/GaAs HBTs (heterojunction bipolar transistors) on germanium-on-insulator substrates having comparable device performance to control structures fabricated on GaAs substrates and bulk Ge substrates. In [38] it is reported on the use of GOI substrates (Soitec production, France) for fabrication of epitaxial InP/InAlAs/GaAs/GOI substrates with further production of chips with HBT and HEMT-like devices. Archer *et al*. [114] used the GOI platform to fabricate GaInP/GaAs double-junction solar cells. Photovoltaic performance of these devices was comparable to those grown on bulk epi-ready Ge.

As a variant, the donor structure is a system of GeSi layers of different composition (gradient layer up to the pure Ge, including GeSi-based stop layer) grown on the Si wafer. Smart Cut™ technology is also used for donor wafer and GeSi layer exfoliation, and the presence of stop layer makes it easier to obtain the planarity of the film bonded to the handle Si wafer [115]. This technique is positive in the thing that the donor Ge/GeSi/Si structure is grown on the Si wafer and, hence, it can have a diameter equal to that of the handle wafer. However, as it was mentioned above, Ge films grown this way on Si wafers have their dislocation density not lower than 10^6 cm^{-2} [49].

Fitzgerald and co-workers, having elaborated the Ge-on-Si growth technology through the gradient GeSi layer, fabricated a number of devices on the base of GaAs grown on such a platform [51, 54, 57, 60]. However, a 10 µm gradient layer did not allow arranging all the elements of integrated circuits based on Si and GaAs optoelectronics simultaneously on one Si wafer. Understanding this, the authors proposed a new Si/Ge/GeSi/Si-like platform having called it SOLES (Silicon On Lattice-Engineered Substrates) [116, 117]. Using standard Smart Cut™ technology, they realised the bonding of a Si thin layer over heterostructure Ge/GeSi/Si. Thus, the upper Si and its under layer Ge are less than 1µm away in thickness. In the windows out etched in the upper Si layer and oxide, i.e. on the Ge surface, high-quality III-V-based heterostructures can be grown, and elements of Complementary Metal Oxide Semiconductor (CMOS) technology can be produced on Si. In [117] the authors demonstrate a working LED's matrix based on heterostructure AlGaInP, grown in the windows of such a platform. They believe that such artificial substrates are one of the ways to realise integrated circuits on silicon with optical connections.

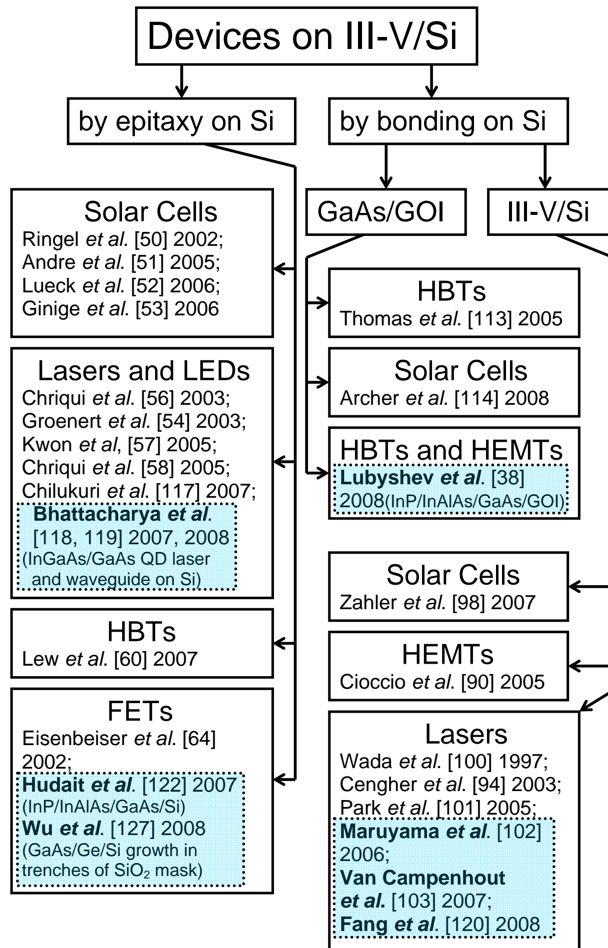

Fig. (8). Publications describing the fabrication of device III-V/Si-type heterostructures and devices on their base grouped according to the character of overcoming lattice parameter misfit between Si and III-V: epitaxial growth or wafer bonding.

4. III-V/SI-BASED DEVICES

Different fabrication ways of device quality GaAs (III-V) on Si wafers are mentioned above, and they can be divided into two trends: purely epitaxial technologies and those whose key element is various methods of bonding crystalline structures with lattices different in their parameters. According to this division, the basic publications in which it is reported on the fabrication of III-V/Si-type device heterostructures and devices on their basis are presented in Fig. (**8**). As is seen from the figure, the main types of devices fabricated on GaAs wafers are also produced on heterostructures whose basic wafer is Si. Heterojunction bipolar transistors, devices working on minority carriers are especially sensitive to structural imperfections of semiconductor materials. Their successful fabrication can be a test for high quality of the heterostructure used for this purpose. Thus, Lew *et al.* [60], having grown a GaAs/Ge/GeSi/Si-type heterostructure using purely epitaxial technologies, fabricated HBTs on them. A maximum current gain of ~100 is reached, which is high enough for microwave applications. The higher leakage current in HBTs on SiGe/Si could be due to the TDs ($\sim 10^6$ cm^{-2}) usually seen in such platforms. At the same time, using

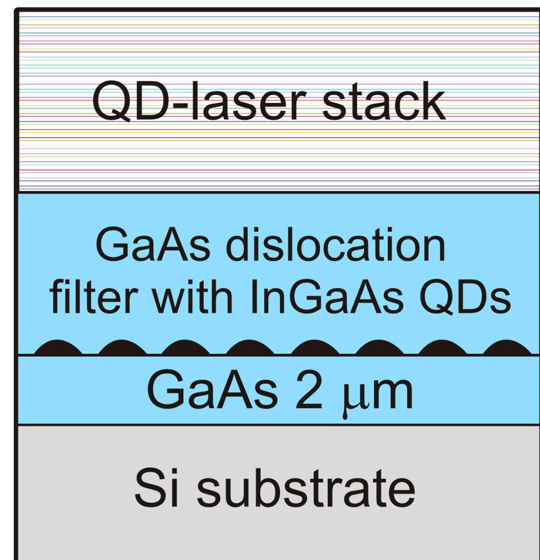

Fig. (9). Scheme of GaAs superlattice-based dislocation filter with InGaAs islands and $In_{0.5}Ga_{0.5}As$ of the quantum-dot laser structure on the Si wafer. By [118].

GOI-based wafers, Lubyshev *et al.* [38] demonstrated transport properties of III-V HEMTs and large area device characteristics for III-V HBTs on GeOI/Si substrates and shown that they were comparable to reference structures grown on InP substrates. The same can be said for lasers: these devices fabricated on the heterostructure bonded to Si have the characteristics close to the standard and even, as it is mentioned in [100], higher output power, due to better thermal conductivity of Si wafer. For lasers fabricated on purely epitaxial GaAs/Ge/GeSi/Si-type heterostructures, the fact of their fabrication proper (as it was mentioned, lasers made on this epitaxial platform were functional not more than 4 hours [55]) is an achievement.

The research papers for the last 2-3 years, in which investigations and elaborations that allowed us to speak about a new developmental era of device technologies based on III-V compounds on Si wafers, are marked in the scheme of Fig. (**8**) by the dotted rectangles. Yang *et al.* [118] used the superlattices of "quantum dots" — InGaAs islands on GaAs to improve the GaAs structure grown with MO-CVD directly on the Si wafer (Fig. **9**). Such structures were of little difference from GaAs films grown on GaAs wafers in their intensity of upper GaAs layer photoluminiscence. The authors presume that the superlattice with strained InGaAs (InAs) islands is an effective dislocation filter. $In_{0.5}Ga_{0.5}As$/GaAs QD separate confinement heterostructure lasers with minimal threshold current 900 A/cm^2 working at room temperature on 1.1 μm wavelength were fabricated on such platforms. In their next paper [119], the authors demonstrate monolithic integration of epitaxially grown InGaAs/GaAs self-organised quantum dot lasers with hydro-genated amor phous silicon (a:Si-H) waveguides on silicon substrates.

Today's computer processors are strictly electronic devices, transmitting data by means of electrons travelling through copper wires. But this technology is relatively slow and produces heat. Now, researchers have developed optical connection nets that could play a key role in replacing elec-

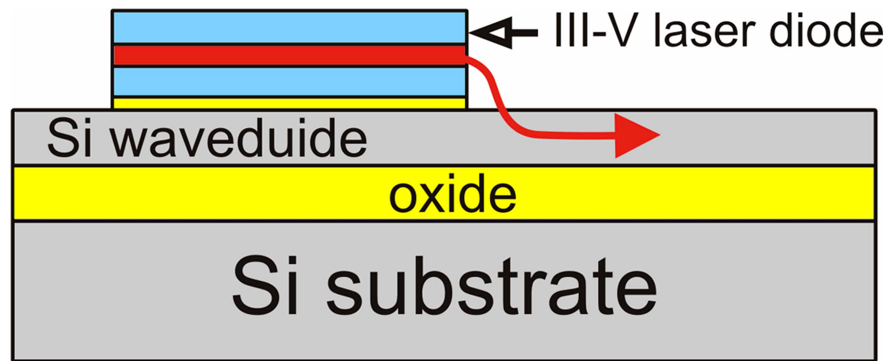

Fig. (10). Scheme of laser diode and Si waveguide assembly on the Si wafer. By [103].

trons and copper wires. Investigations in this direction are scope of activity of Si photonics.

Since Si films on insulator substrate can be used to fabricate compact optical circuits as waveguides, integrations of photonic devices such as lasers, optical amplifiers, electro-absorption modulators, etc. on SOI platforms are very attractive. Integration of laser diodes and silicon waveguides on the Si wafer by bonding is demonstrated in a number of papers [101-104, 120]. Thus, in [103, 104] the authors demonstrate the electrically injected wave lasing in InP-based microdisk lasers, fabricated through heterogeneous integration of InP on SOI and coupled to a sub-micron silicon wire waveguide. The laser emits at 1.6 µm, with threshold current as low as 0.5mA under continuous-wave operation at room temperature and threshold voltage of 1.65 V.

The scheme of a microdisk laser InP/InAsP-based structure integration with a SOI waveguide circuit is presented in Fig. (**10**). A microdisk is the part of a thin InP-based layer bonded on top of a SOI wafer. As the authors assert, to fabricate these photonic integrated circuits, standard CMOS technology can be used. An electrically pumped distributed feedback evanescent laser fabricated on the base of InP is proposed for the same purposes in [120]. The III-V epitaxial layers are transferred to the patterned SOI wafer through wafer bonding at 300 °C.

In [38, 121, 122], new approaches to the creation of device base for III-V compounds on Si wafers, based on solid solutions close to that of InP are demonstrated. As is known HBT- and HEMT-type devices fabricated on the base of InP and on InP wafers are of the fastest operation due to high mobilities of electrons in III-V compounds with band gap width less than 1 eV. Maximum oscillation frequency 755 GHz was achieved [123]. Earlier, successful attempts had been made to replace a more expensive InP wafer by GaAs (see. e.g. [124]). The gradient transfer over GaAs lattice parameter towards InP was realised based on the AlInAs solid solution of variable composition [125]. It turned out that such a buffer layer, 1µm thick only, is sufficient for growing perfect heterostructures and fabrication of efficient HEMT-type devices [126]. Later researchers from IQE Inc. found that such AlInAs-based buffer layer is an effective filter of dislocations if it is grown over GaAs-on-Si wafers. Characteristics of FETs carried out on platform AlInAs/GaAs/Si presented in [121, 122] open new prospects for high-speed digital logic applications, and the total buffer AlInAs/GaAs layer thickness, not more than 1.5 µm allows us to apply CMOS technologies. Logical is these authors next step in fabrication of fast operation devices on Si wafers, - namely, replacement of epitaxial GaAs/Si structure by GOI platform with further GaAs growth on it, buffer InAlAs layer and then the InP-based junction for HEMT- and HBT-type device fabrication [38]. The authors used GOI substrates by Soitec on which device quality III-V heterostructures were grown, and devices exhibited dc parameters close to reference HBTs were grown on InP substrates.

A new way to largely reduce the TD density in heteroepitaxial films (Ge or GaAs) grown on Si was demonstrated in [127]. Authors used specific selectively growth in trenches of 200 nm width etched through a thick SiO_2 masking layer. Because of the trench aspect ratio (depth/width) was more than 1, threading dislocations originating at the Ge/Si or GaAs/Si interfaces terminated at the oxide sidewalls. Fig. (**11**) shows the sequence of epitaxial growth of Ge in trenches on Si. Defect trapping was achieved within 200 nm of the Si surface. After coalescence of Ge crystals and their chemical-mechanical polishing the GaAs film of a high quality could be grown. Depletion-mode Al_2O_3/GaAs MOSFETs were manufactured on such platform [127].

The point of introduction of GaAs and III-V compounds as elements of silicon CMOS integrated circuits remains unclear. Elaborations of new integrated circuit generations come across the problem of "restriction in size reduction of certain circuit elements with used materials": Si forming the traditional transistor and capacitance, SiO_2 and polysilicon, - with their size reduction, - reached fundamental physical limits closing to the 100 nm technological node. The ongoing chip elements decrease requires the introduction of new materials in silicon integrated circuits, necessary to intensify transport properties of transistor channel in CMOS integrated circuits and, respectively, preservation of developmental rate according to Moor's law. On the prognoses formulated in the International Technology Roadmap for Semiconductors (ITRS) 2007 [128], Ge and also III-V compounds could be such materials. The prognosis is based on the fact that the main III-V compounds have a considerably higher electron mobility compared to that of Si. Carries mobility can be increased additionally by strains.

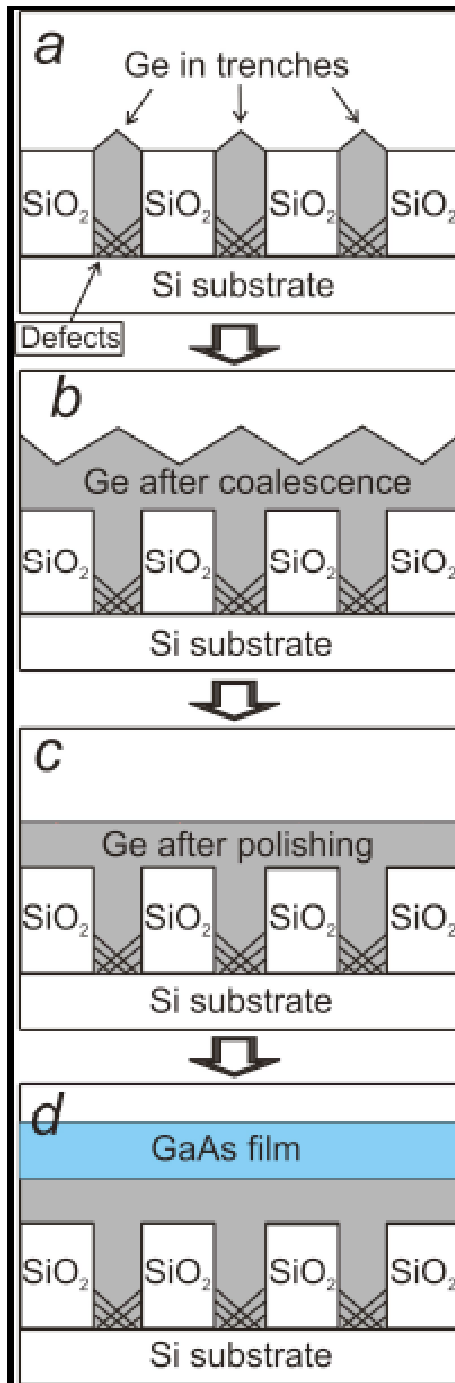

Fig. (11). Cross-sectional schematic view of the GaAs/Ge structure grown on Si. (**a**) – Ge micro crystals grown in trenches of SiO_2 mask; (**b**) – coalesced Ge film; (**c**) – Ge film after chemical-mechanical polishing; (**d**) – GaAs film grown on top of Ge. By [127].

As is indicated in the review by Takagi *et al*. [129], III-V channel transistors for n-MOSFETs and Ge channel for p-MOSFETs are considered as one of the prospective combinations for fast operation devices. However, despite the vivid profit in the introduction of III-V as a material for the channel with high carrier's mobility, constructive ways of such an introduction are still not clear. The impossibility of epitaxial deposition for ultra-thin, but low defective GaAs films and other compounds on Si — due to earlier indicated reasons — is a considerable, yet not overcome, barrier. The complications are the necessity of different materials for p- and n-type channels, various most rational channel directions in a crystalline lattice and different strain character (compression — tension) for these channels [129-131]. Because of the necessity to fabricate p-MOSFETs with a channel from another material (e.g. Ge) on the same Si wafer, researchers come to the conclusion that III-V compounds will, probably, be selectively introduced onto Si wafers [132, 133]. Thus, the [133] review authors write: "Due to reduced dimensions.... the extended defect concentration can be reduced as the film dimension in at least two dimensions would be very small. To reiterate, if the conventional Si channel could be replaced by a GaAs channel, the MOSFET operation speed can be improved greatly". However, even in channel size reduction down to several tens of nanometers, GaAs nucleation in its epitaxial growth on Si will proceed as it was shown earlier, - namely as separate islands. According to Asai *et al.* [15], ~10 islands on the area 100×100 nm^2 form at the earliest film growth stage. Just before their coalescence, islands become dislocated. So far there are no grounds to presume the thing that the island character of GaAs-on-Si initial part of growth will be overcome with dislocation density reduction down to not more than 10^6 cm^{-2} in a completely relaxed GaAs film. It is significant to note that the linear density of edge misfit dislocations which are necessary to compensate the lattice parameter difference between GaAs and Si, is ~100/µm and they inevitably are in the GaAs/Si interface and close to it. Contrary to epitaxial growth the way of GaAs bonding with Si wafers is virtually free of that kind of defects.

5. SUMMARY

For the last more than 20 years researchers have been trying to integrate Si- and III-V-based devices on the most efficient silicon wafer. Two ways of overcoming the main barrier in the successful integration of III-V-based devices on Si wafers with a 4%- and more lattice parameter difference between them have outlined for the last several years. It is a purely epitaxial growth using gradient buffer layers and different dislocation density reduction techniques: annealing, dislocation "filters", special regimes of GaAs-on-Si initial growth steps. Another way — bonding III-V compounds and III-V-based heterostructures on silicon wafers or using GOI (germanium-on-silicon-insulator) substrates - becomes more popular in connection with the development of various non-epitaxial integration methods for two heterogeneous semiconductor materials.

The main advantage of epitaxial growth consists in that the Si wafer is the only one used in this technology. However, because of a high lattice parameters difference III-V and Si, it is possibly to grow relatively perfect GaAs (and other III-V) films with dislocation density not lower than $10^6 cm^{-2}$, which is insufficient for long operation of certain type devices (lasers, photodiodes). Big distance in thickness between GaAs and Si surfaces exceeding 10 µm, in case of using gradient baffer Ge/GeSi/Si layers, is a considerable barrier for high resolution lithography methods for connections between Si and III-V neighbours on the substrate.

Non-epitaxial bonding methods give a new degree of freedom and enable us to make new combinations of materials that could not be realised earlier by epitaxial growth. Thus, a big number of defects, inevitably appearing in the film under heteroepitaxy, is absent under the transfer by bonding. Herein, it turns out possible to fabricate such structures, in which GaAs (also other III-V compounds) and Si are directly close to each other, and this is one of the key factors for integration of silicon integrated circuits and GaAs optoelectronics on one silicon wafer.

The results achieved in device application of III-V-on-Si can be characterised in a different way depending on the earlier set aims:

-Replacement of GaAs and InP wafers for Si to fabricate III-V-based semiconductor devices on a cheaper, bigger-sized, bigger strength and higher thermal conductivity Si wafer. Several solutions were proposed: high temperature anneals and TCA of epitaxially grown GaAs/Si heterostructures, epitaxial transition from Si through buffer GeSi layers to Ge (and then GaAs growth), using buffer AlInAs layers to InP-related heterostructures, involving a new GOI wafer or GaAs/Si and InP/Si wafers fabricated by wafer bonding. III-V-based devices: lasers, solar cells, HBTs, HEMTs and QWFETs are fabricated on such artificial wafers.

-Integration of devices based on III-V compounds and silicon planar technology on the Si wafer. Examples for the beginning of such integration — InP-based lasers and silicon waveguides, AlGaInP-based photodiode matrix arrays and contacts to them, realised using CMOS technology - were demonstrated.

-Acceleration of CMOS integrated circuits fast operation through the replacement of Si channels in FETs by those with higher electron mobility based on GaAs (InGaAs). Despite the vivid profit in the introduction of III-V compounds as a material for a channel with high mobility of electrons, constructive ways of such an introduction are still not clear.

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