Perspectives of Overdamped Josephson Junctions in Voltage Standard Applications

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Abstract: We discuss the main characteristics that must be satisfied by Josephson junctions for metrological applications and, specifically, in the development of voltage standards of new generation. Data reported in the literature for the most established technologies, like SNS (Superconductor-Normal conductor-Superconductor), SINIS (Superconductor-Insulator-Normal conductor-Insulator-Superconductor) and others, are analyzed and compared. The properties of Nb/Al-AlO_x/Nb overdamped SNIS (Superconductor-Normal conductor-Insulator-Superconductor) Josephson junctions developed at INRiM are also presented, since these junctions can optimize crucial parameters such as the current density and the characteristic voltage. Operation at temperatures above 4.2 K is also discussed, in view of using cryocooler setups to replace liquid helium refrigeration systems.

1. INTRODUCTION

Josephson junctions used nowadays in DC voltage standard applications are based on hysteretic SIS (Superconductor-Insulator-Superconductor) junctions with zero crossing steps, i.e. voltage steps whose current range spans positive and negative values, including the condition of zero DC bias. The choice of this technique dates back to the first attempts in series-connecting the thousands of junctions needed to reach output levels of 1 V and above, as required in metrological applications. Exploitation of the zero crossing steps, fist suggested by Levinsen [1], eventually allowed to overcome many technological difficulties and made it possible to realize arrays with reproducible overlapping steps, providing DC voltages up to 10 V. The availability of 10 V standards with quantum accuracy has led to dramatic improvements in DC voltage metrology, and it is now possible in primary DC voltage calibrations at 10 V to attain relative uncertainties as low as 10^{-11}.

More recently, the interest in voltage standard research has moved to the investigation of techniques for extending the application of Josephson arrays to AC quantum standards and to standards for arbitrary time-varying signals. To this aim, junctions with non hysteretic behavior were suggested to allow changing the output voltage through control of the bias current. The substantial difference, from the application viewpoint, in using non hysteretic junctions, is that their IV curve (voltage *vs*. current relationship) under irradiation is a one to one staircase, thus the output voltage is univocally defined by the current feed through the bias circuit. This is not the case for hysteretic junctions used in DC standards, were steps are overlapping and all share approximately the same interval of currents.

In the so-called programmable standards, the junctions bias currents are used to activate/deactivate array sections. Such arrays are typically subdivided in sub-circuits with series connected junctions generating voltages following a power of two sequence (see Fig. **1**). Combining the sections it is then possible to source binary programmed voltages in a way that is very similar to the technique used in electronic digital to analog converters [2]. In order to replace best AC standards, the uttermost accuracy has to be reached and many efforts have been devoted in realizing arrays with performances suited to the tight requirements set by modern primary metrology. Many approaches to junction fabrication have been developed, and several different technologies have proven successful in providing voltages up to 10 V, with good metrological properties. Programmable Josephson arrays are so far the most successful attempt to extend metrological applications of Josephson standards beyond dc. Programmable arrays operating at 1 V have been effectively used for several applications: as traveling standards for international comparisons [3], for generating precisely varying voltages in a watt balance [4] as quantum impedance and power standards [5]. Moreover, only programmable standards can presently provide output voltages up and above 1 V, and even exceeding 10 V [6].

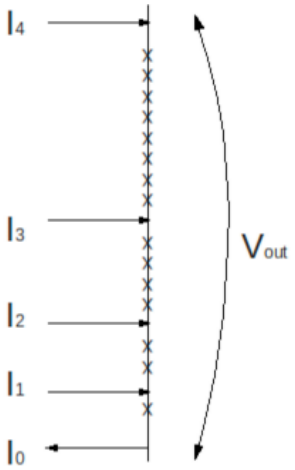

Fig. (1). Operating principle of programmable Josephson arrays. By controlling the bias currents I_1-I_4it is possible to change the output voltage V_{out}.

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Nonetheless, this technique suffer from some limitations, the most severe is due to the time for step switching, where junctions are not operating in a quantized state. During these transients, the array voltage is not precisely known and the uncertainty of the generated signal increases with the fraction of period spent in the transients. Since the minimum transient time is constrained by technological limitations, programmable arrays can fulfill primary metrology uncertainties only for signals with frequencies up to few hundreds Hz [7].

To overcome limitations of programmable standards, arrays operating with a pulsed, square wave, rf signal have been developed. Using short pulses instead of a sinusoidal rf signal makes it possible to effectively modulate the signal period while keeping junctions phase locked over a wide range of frequencies [8-10]. Fundamental accuracy follows from the control of the flux quanta transferred through the junctions by the pulsed signal. The output voltage is then exactly calculable in terms of fundamental constants if the number of the flux quanta per unit time, i.e. the pulse repetition rate is known [11]. Pulsed standards allow to synthesize arbitrary waveforms with quantum accuracy based on the sigma-delta technique for digital to analog conversion developed for semiconductor electronics and very high spectral purity [12]. Both operation and fabrication of pulsed standards set very challenging problems. Due to the complexity of pulse waveform, the apparatuses for generation of precisely frequency controlled pulses are sophisticated and expensive, and the design of rf transmission lines is extremely difficult because of the harmonic richness of the signal. In addition, it is extremely difficult to generate a bipolar output with a frequency modulated Josephson array, and very complex AC biasing techniques, involving a sine wave and a pulsed signal, both synchronized, must be used for real AC operation [12]. Generation of the pulse train for proper junction operation requires top-end instrumentation and unavoidably limits the signal fundamental frequency to values much lower than those obtainable with continuous wave sources. Power distribution to array junctions is also of concern, since the usual microwave techniques developed for nearly monochromatic signals are not directly applicable to broadband pulses. Adoption of lumped circuit methodologies seems at present the most viable solution, though highly demanding on the fabrication side. In order to have negligible effects on circuit behavior, the propagation time of rf signal along the array must be smaller than the signal period, i.e. the array dimensions must be smaller than the signal wavelength λ. To guarantee reliable operation, $\lambda/8$ is typically considered the maximum value acceptable for array dimensions [13]. Despite all these difficulties, arrays with as many as 10000 junctions have been successfully fabricated, providing synthesized voltage signal exceeding 200 mV, with quantum accuracy and extreme spectral purity [13].

A new technique has been recently proposed to overcome some of the difficulties encountered with programmable and pulsed standards. The method, named Pulse Power Modulation (PPM), is based on a controlled activation/deactivation of the driving rf signal, to simultaneously set every junction in the array into either one of two states: zero voltage in absence of rf signal and a quantum defined step voltage upon rf application. Waveform synthesis can then be realized by Pulse Width Modulation of the array voltage [14]. The requirements in junction technology for PPM are different form those set by programmable and pulsed standards, since for proper operation an IV curve where the interval of currents of the relevant steps partially overlaps the critical current is needed. Such a behavior can be obtained if a precise control over junction hysteresis is feasible in the fabrication stage, to provide an intermediate degree of hysteresis, between those of the fully hysteretic SIS for DC and the non hysteretic SNS.

Although limited in space, this overview wouldn't be complete without mentioning RSFQ (Rapid Single Flux Quantum) as an alternative technique to synthesize arbitrary and AC signals with quantum voltage accuracy. RSFQ has been, and still remains, a very active field of research for quantum digital electronics applications, yet developments for voltage standards have always been left out of the mainstream of research interests in Metrology [15]. One of the main reasons for that is most likely to be found in the completely different approach, know-how and experiences involved by RSFQ, with respect to the common background of voltage metrologist. In RSFQ standards, accurate voltage signals are generated by controlling flux quantized by a Josephson junction. Flux quanta generation is "triggered" by a pulse sequence, thus can be precisely timed, in analogy with the "phase lock" process exploited in array standards [16]. RSFQ approach is potentially advantageous in that the complex and expensive microwave apparatus needed for ordinary standards is avoided, the drive signal being generated by the superconductive circuit itself. The only requirement for RSFQ circuits is an external accurate frequency reference, typically operating in the MHz range. The simplification in instrumentation must be traded off with a much higher complexity of superconductive circuit, namely an increased number of junctions, additional elements like inductors, and fabrication of junctions with different parameters in the same device. The basic element in RSFQ is the Josephson transmission line, a string of Josephson junctions connected by inductors where the pulse can propagate, like in transmission lines, and even amplified [17]. A basic Digital to Analog converter suitable for voltage standard will include at least some voltage multiplier stages, to increase the output signal to practical values (See Fig. **2**). Coupling between Josephson transmission lines and voltage multipliers is obtained by capacitive coupling [18], but magnetic coupling through transformer-like circuits has proven to be more effective [19]. Nowadays DAC for Metrology are fairly more complex devices, with many digital blocks performing various specialized functions, and correspondingly high power consumption. Successful operation, of a 10-bit RSFQ DAC capable of generating up to 20 mV has recently been reported [20].

2. CURRENT JUNCTION TECHNOLOGIES AND FABRICATION ISSUES

The fabrication of arrays for AC generation and waveform synthesis is a difficult, challenging task, and many different technologies have been proposed and tested, yet the choice of material and fabrication techniques still represents an open question. Independent of the technique adopted for signal generation, a relevant problem is posed by the high

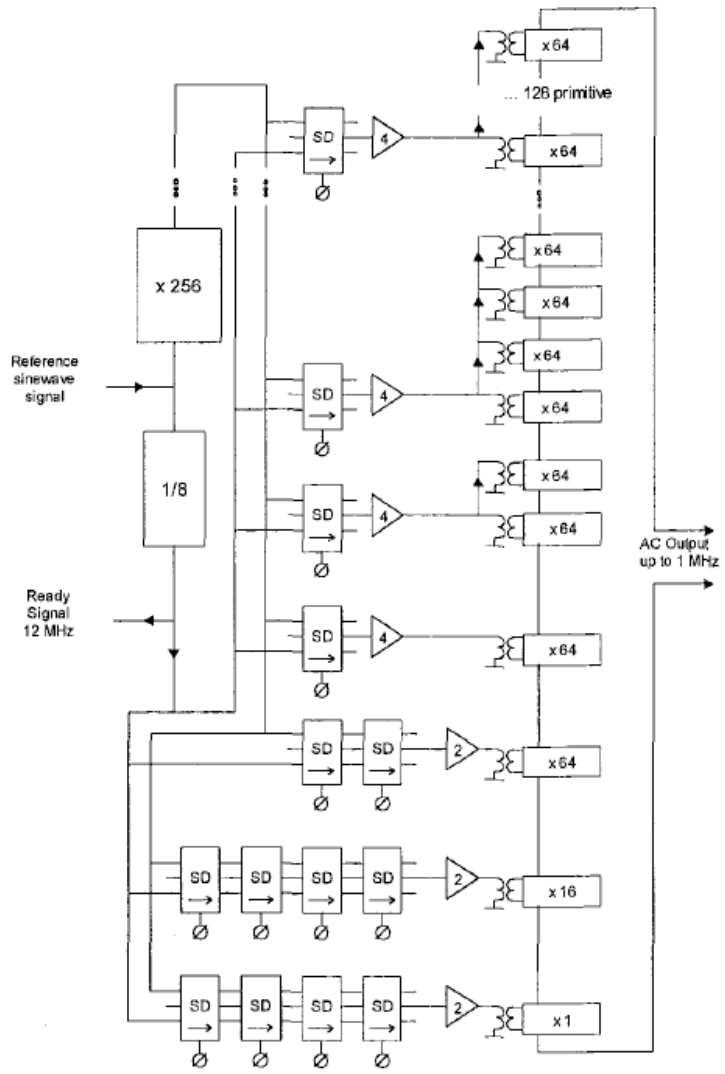

Fig. (2). Simplified schematic of a Digital to Analog converter realized with RSFQ technology (from [16]).

number of junctions needed to reach practical voltages, since junctions for AC typically operate on the first step and the drive frequency is limited for technical and economical reasons [21]. A high noise immunity, low power dissipation, reduced dimensions are also essential properties in metrological applications and in view of spreading quantum standards to a wider range of users.

The chip dimensions are set by the area and the number of junctions, both essential parameters for technology, because a reduced area along with a high number of junctions make it difficult to guarantee the uniformity of their electrical properties, which is essential to observe decent collective steps.

These requirements can be translated into well-defined specifications on junction parameters. First, the critical current I_c, that sets an upper limit on the amplitude of the quantized steps, should be large enough for steps with suitable width and noise immunity, yet a too high value increases dissipation in junctions. The area of the junction must be small, to reduce array dimensions, but avoiding the excessive difficulties in fabrication imposed by deep submicron patterning, today still hard to achieve for high integration superconductive circuits. It follows that an optimal range exist for critical current density. Presently, values ranging from 10 to 100 kA/cm^2 appear to be the best choice.

The characteristic voltage $V_c=I_cR_N$ with R_N junction normal tunneling resistance, determines the microwave optimal drive frequency f_d, from the relation $\Omega = f_d / f_c$, where $f_c=(2e/h)\,V_c$ and thus the step voltage (i.e. the voltage resolution of the array) and the number of junctions needed to achieve the maximum requested voltage output. To obtain the maximum step amplitude, Ω must be ≈ 1 [22]. In order to use commercial microwave instrumentation and reduce as much as possible the number of junctions, drive frequencies close to 70 GHz are used, and V_c around 150 μV are needed. Of course even larger values, which on the other hand are absolutely advantageous for speed applications, can be used. But in voltage standard application this causes a sensible reduction of the step width.

The characteristic voltage defines also the highest speed of RSFQ circuits since this is proportional to $\tau_c=1 / f_c$, In this case, the highest V_c and the higher the speed.

A challenging problem to be solved in the next future for voltage metrology and superconductive electronics applications, is operation in cryocoolers at a temperature greater than 4.2 K. Indeed, in order to make the Josephson quantum standards available to a widespread market, rather than limited only to the National Laboratories, as well as affordable for private companies needing an accurate voltage reference, refrigeration systems cheaper and more compact than those nowadays used for niobium junctions are required.

At present, however, large arrays fabricated with higher critical temperature superconductors like YBCO (Yttrium Barium Copper Oxide), or the more recent MgB_2 are not yet available, since the technology of these junctions do not allow to achieve the required integration level [23, 24]. The best results have been achieved by shunted bicrystal YBCO junctions, where voltages near to 30 mV have been measured at 77 K [23].

Therefore in this paper we discuss extensively niobium and niobium nitride based junctions, considering high T_c junctions in the section devoted to the use at temperatures above 4.2 K.

Considering the electrode configuration, non-hysteretic IV characteristic can be obtained by three main classes of junctions:

- hysteretic SIS with external shunt
- metallic barrier SNS
- double barrier SINIS

The first class, directly derived from the most developed and optimized process of superconductive electronics, and which is still the predominant technology for RSFQ circuits, suffers from the disadvantage of a configuration requiring an external resistor or a more complex circuitry. This, with the severe limitation to *Ic* from chaotic instabilities [25] limits the use of these junctions in voltage standard circuits. Therefore we will not consider junctions of this type in the following, where a detailed analysis limited to the last two classes will be carried out.

2.1. Programmable Voltage Standards

Programmable voltage standards (PJAVS) are made with series-connected subarrays, whose size follows a power of two sequence. Through control of the bias current of each section, the series voltage is set by the code represented by on/off status of array bias lines. To switch subarrays, junctions that can generate a current-controlled, univocally defined voltage, i.e. junctions with a single valued (non-hysteretic) IV curve must be used. To provide signal to noise ratios adequate to metrological applications, critical currents at the mA level are at least required. On the other side, due to the fact that only the first Shapiro step of junctions is used, to achieve voltages of 1 and 10 V, V_c even in excess of 100 μV are sought to reduce number of junctions.

As known, the amplitude of the n = 1 quantized Shapiro step normalized to the critical current attains its maximum when the microwave drive frequency and the junction characteristic frequency are nearly equal. This corresponds also to a condition of minimal power dissipation [22]. This leads to optimal $V_c$of 100-200 μV.

SINIS junctions achieve the shunting of the capacitance of a SIS junction, by using two, very thin oxide layers, separated by a metallic barrier. They are typically made of Nb/$Al/AlO_x/Al/AlO_x$/Al/Nb and have been extensively studied both theoretically and experimentally [26-30]. The best results on these junctions for superconductive electronics applications and especially for programmable voltage standard have been obtained by the PTB group, who realized complete successful circuits for programmable potentiometer at 1 and 10 V level with 7000 and 70.000 junctions respectively. These SINIS junctions feature $J_c \leq$ 1 kA/cm^2, V_c as high as more than 250 μV at 4.2 K with junction size 100-1000 μm^2 [31]. SINIS junctions with various values of Al thickness and AlO_x barrier transparency have been reported, but, even if feature J_c and V_c higher than those given above, their IV characteristic was rather anomalous showing an high residual hysteresis at 4.2 K, and they were hardly reproducible [32, 33].

In general a problem for the SINIS junctions is due to the high transparency of the two insulating barriers, with the necessity to realize very smooth planarization of the underlying films, since the probability of defects such as pinholes is increased. The fabrication process, requiring two barriers and three thin aluminum layers highly homogenous, has limitations for the fabrication of really high number of junctions, as in arrays for programmable voltages operating at 10 V and more [34].

In SNS junctions the damping of the IV characteristic for non-hysteretic behavior is obtained by using a normal metal as barrier. SNS have high values of J_c, but typically the metals used have very low resistivities. Nb/PdAu/Nb junctions have been the first developed type of SNS junctions for this application by NIST group, and have produced stable voltage outputs at 1 V as binary arrays for programmable potentiometers, being also used in circuits for pulse driven AC synthesis [11, 12]. They feature values in the range of 100 kA/cm^2 and V_c between 5 and 30 μV with typical size of few μm^2, even if $J_c$values would support also submicron dimensions. The values of V_c limit their use to drive frequencies of few GHz.

Impressive results have been obtained with NbN/TiN/NbN junctions, developed by the Tsukuba group, since very large arrays, with more than 300.000 series connected junctions have been successfully tested in a 8 and 11 bit DAC circuits with quantized steps at 10 V at 10 K [35, 36]. Features of these junctions are J_c about 10^4 A/cm^2 and V_c 10-20 μV at 10 K, with areas of few square micrometer.

Materials have been also proposed as normal metal barrier which are at the metallic insulator transition. In such a way it was possible to tune the barrier resistivity and the characteristic voltage of the junctions [37, 38]. Among the experimental results we mention Nb/TaO_x/Nb, NbN/TaN/NbN and Nb/Nb_xSi/Nb junctions. Nb/TaO_x/Nb junctions fabricated at IEN-INRiM, showed resistivities varying different order of magnitudes depending on the bias voltage of the cathode during the sputtering deposition of the TaO_x film [39]. The junctions have however a marked aging, featuring a reduction of at values less than 10 A/cm^2. Also NbN/TaN/NbN junctions studied in [40] have not yet been suitable for large circuits production. These junctions featured very high V_c, up to more than 0.5 mV at 4.2 K with

$J_c 10^4$-10^5 A/cm^2, but required a difficult tuning of fabrication parameters and also the temperature dependence of these parameters was critical.

In this category, Nb/NbxSi/Nb junctions represent the most successful attempt sofar. Although previously studied by Barrera and Beasley in the '80 [41], the most promising results have been achieved recently by the NIST researchers, which experimented these junctions in multistacked arrays [42]. These authors achieved a transition from a conductive to an highly resistive phase by varying the sputter deposition power of the two elements. J_c varying from 10 to 10 kA/cm^2 and V_c from few μV to 150 μV and more at 4.2 K have been obtained. Outstanding results have been obtained within a cooperation between NIST and PTB [34], that jointly realized a programmable 10 V array with about 70,000 junctions.

The stabilization of the barrier stoichiometry, critical aspect of this type of junctions, can be achieved by a thermal annealing after the deposition of the trilayer [43].

2.2. Pulsed Standards for Waveform Synthesis

The series of pulses used for waveform synthesis has a very rich harmonic content and requires proper optimization of the microwave behavior in circuits for rf signal distribution. Most of the techniques adopted for analysis and design of circuits with distributed parameters assumes operation with narrow band signals, thus cannot be directly applied for pulse transmission. The most reliable solution to guarantee pulse operation is to reduce array dimensions allowing lumped analysis of circuit. To that aim array length must be shorter than λ/8, where λ is the wavelength of the microwave signal. This constraint sets strong requirements on junctions technology, in particular on junction size. In order to realize the array configuration described, materials resulting in improved steepness of the etch profile are preferred, especially when multi-stack junctions are employed.

SINIS junctions, initially developed for programmable voltage standards and previously described, have also been used for AC synthesis [28].

Nb/HfTi/Nb junctions have been experimented by PTB team with successful results in the realization of large submicrometric circuits for AC synthesis which have recently reached quantized voltages from 2000 series junctions [13]. These junctions feature about 80 kA/cm^2 for HfTi 20 nm thick and of 15 μV in 0.2 μm × 0.2 μm junctions.

SNS junctions with similar low characteristic voltage, such as Nb/Ti/Nb junctions developed by Jena team and Nb/Al/Nb junctions studied at INRiM have not been resulted in large circuits yet [39, 40]. Ti barrier junctions feature j_c of 10^4-10^5 A/cm^2 and V_c from 10 μV up to 100 μV, while for Al film 100 nm thick, also higher values of and similar or lower values for were obtained. In both case the junction size was in the micrometer and submicrometer range.

Nb/MoSi/Nb junctions also studied and experimented by NIST team, have been used to realize multistacked junctions for lumped arrays for AC synthesis [43, 44]. They feature critical current density between 10^4 and 10^5 A/cm^2, depending on barrier thickness, so that can be increased up to 200 μV in junctions of few μm^2.

2.3. Power Control Standards

Power control standards set some peculiar requisites on junction technologies, their operation being based on the overlapping of the range of currents of the steps and critical current. To fulfill these requirements, a tight control of junction hysteresis is needed.

Referring in particular to [45], where the junctions parameters for the overlapping of the n=0 and n= 1 step are reported, it is pointed that the mentioned overlapping is obtained in a stable way when $f > (1.5\text{-}2)\ f_c$. In particular the authors suggest the adoption of edge type junctions with V_c as high as 1 mV. However, in principle, no constraint on V_c is needed, while the need of a sufficient, but not exceedingly high overlapping of the two steps is the only fundamental aspect.

First experimental results have been reported for SINIS junctions [46].

2.4. Application to RSFQ

The application of superconductive technology to RSFQ requires a high level of reliability, suitable for the development and testing of very complex circuits, with thousands of junctions implementing many different functional blocks. The best established technology, well mastered by many foundries, is based on SIS junctions, usually made of a Nb/AlO_x/Nb, with an externally shunt resistor [47]. The minimum junction area that can be fabricated with this technology is 12 um, and the whole process involves as many as 12 mask steps. Impressive results have been obtained with the standard Nb/AlO_x/Nb technology: in [48] the operation of a RSFQ quantum DAC with 6000 Josephson junctions, subdivided in several functional blocks, is reported. SINIS junctions have proven to be suitable for RSFQ, and some fundamental circuits based on this technology were successfully operated [49]. More recently, owing to the wide range of tunability of their electrical parameters, co-sputtered Niobium-silicide barrier junctions appear interesting for a wide range of applications in digital electronics and well suited to RSFQ [50].

3. NB/AL-ALO_X/NB OVERDAMPED SNIS JUNCTIONS

3.1. Structure and General Properties

Overdamped junctions developed at INRiM can be seen as an extended case of hysteretic Nb/Al-AlO_x/Nb SIS junctions, where the thickness of the Al, is increased up to 30-100 nm instead of the typical 5-10 nm, the oxidation dose being in the range 50-500 Pa·s. The niobium electrodes are 100-200 nm thick and the patterning of the base and top geometry is performed by lift-off and RIE respectively. Insulation *via* liquid anodization and deposition and patterning of the wiring layer are carried out accordingly to previously described recipes [51].

These junctions can be described as SNIS, since the thick aluminum film is a normal metal at liquid helium temperature. However, an essential feature is that, at 4.2 K, a transition from the hysteretic to the non-hysteretic state can be induced, when the aluminum thickness is in the above

mentioned range, by changing the AlO_x exposure dose. Conversely, once chosen Al thickness and AlO_x exposure values, this transition is observed as function of the junction temperature in measurements below 4.2 K [52].

A feature of overdamped SIS junctions of interest both in metrological applications and for high speed devices is the high value of current densities achievable, up to 10^5 A/cm^2, along with V_c up to several hundreds microvolt at 4.2 K. Junctions with Al thickness ranging from 70-100 nm and exposure doses of AlO_x between 150 and 250 Pa·s show j_c from 10 to 25 kA/cm^2 and V_c up from 0.1 up to 0.5 mV at 4.2 K.

Good overdamped junctions have been realized also with 50 and 30 nm of Al. In this case even higher values of and have been measured, by using oxidation exposures from 100 to 500 Pa·s. The dependence of the critical current density and the characteristic voltage on the two mentioned fabrication parameters is shown in Figs. (**3** and **4**).

While data show a regular dependence of J_c on the exposure dose, a less defined dependence for this parameter on the alunminum thickness has been observed in the range from 30 to 100 nm (Fig. **3**). On the contrary, the characteristic voltage of these junctions is strongly affected by aluminum thickness, with and evident linear relationship (see Fig. **4**). The experimental data seems however to indicate

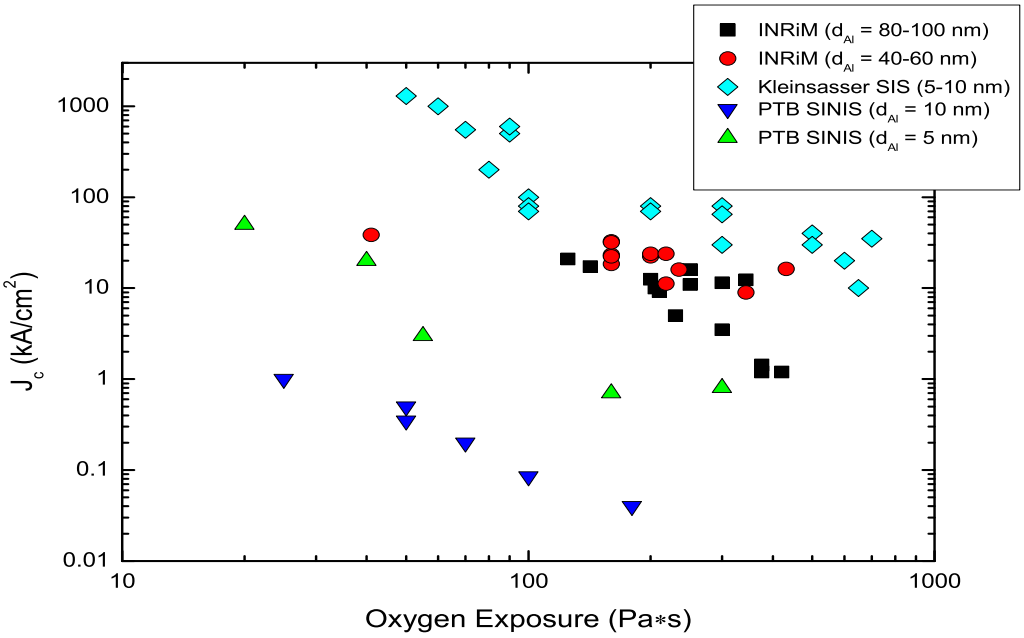

Fig. (3). Dependence of the critical current density on oxidation exposure. Square symbols indicate data corresponding to Al thickness 50 nm, circles are data corresponding to junctions with Al thickness > 50 nm.

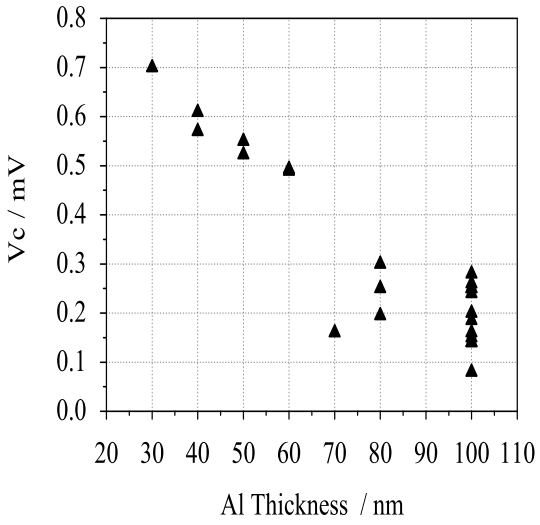

Fig. (4). Dependence of the critical voltage on Al thickness. Circles indicate data observed on junctions with oxidation exposure < 200 Pa·s, square symbols are used for data corresponding to exposures in the range 200-300 Pa·s, and triangles are results obtained with exposures 300 Pa·s.

that there is defined range of thickness of this layer where both and are maximized. A reduction of the aluminum film thickness is indeed desired, since, for instance it affects the transition temperature to the normal state of these junctions: it changes from 7.5 K for a 90-100 nm Al film up to about 8.9 K for a 30-40 nm film. Yet, anomalies of the current voltage characteristic are more easily observed for the thinner aluminum films, since high values and conditions at the border of the hysteretic to non-hysteretic transition results in more pronounced thermal instabilities of the IV characteristic.

Possible interpretations of the shunting of the thin oxide barrier must take into account several aspects. It is well known that the damping of the current voltage characteristic of a Josephson junction is defined by the value of the Stewart-McCumber parameter (see e.g. [53]): $\beta c=(2e/\hbar) I_c R_N^2 C$.

This can be also rewritten as $\beta c=\pi \Delta r Ncs/\hbar$ where c_s is the junction specific capacitance, r_N the junction normal resistivity, related to the barrier This parameter for our junctions is < 1 at 4.2 K, but close to unity.

In general, for different junctions configurations the product of the elementary charge *e* and the characteristic voltage V_C is proportional to the energy gap value of the superconducting electrodes. The usual way to decrease is to reduce R_N, that is to use ultra high transparency barriers. In [53] the replacement of Nb with Al was suggested to reduce the superconducting gap, effectively decreasing the Stewart-McCumber parameter. Our junctions are not made with Al as an electrode material, since, as mentioned, for most of superconductive elctronics applications Nb is preferred, nor have such extremely thin barriers as in [53], thus the risk of pinhole defects is reduced, rather the gap value can be reduced with temperature.It should be noticed that even in the case of the presence of a pin hole, its effect is reduced by the presence of an additional normal Al interlayer that transforms the problem from a direct contact between the electrodes to an SNS region in parallel with the main SNIS.

Indeed our junctions, having not quite high transparency oxide barriers, look also similar in behaviour to the so called metal-to-insulator transition barrier junctions [54], and can be tuned to the hysteretic non hysteretic transition. In any case it seems that an important role is also played by the proximity effect since the thick aluminum film affect the Nb/Al system at the interface with the oxide barrier.

3.2. Reproducibility of Junctions Parameters, Temperature Behavior

The reproducibility of these parameters has been tested by comparing data of 29 different devices belonging to 11 different fabrication wafers. Each wafer had an aluminum thickness of 50 nm ±5%, while the oxidation exposure *Eox* was 200 Pa·s ±25%. Both the wafer-to-wafer and the on-wafer reproducibility have been measured. The overall average characteristic voltages measured at 4.2 K of both single junctions and small arrays are given in Table **1**, along with the values of measured critical currents.

The principal cause of wafer to wafer reproducibility limitation arises from the spread in oxidation conditions, since the described process is presently not automated. As for the oxidation exposure, we use a dynamic process, where the introduction of oxygen flow at an initial pressure of Pa, monitored by vacuum gauge. The on wafer reproducibility is affected by resolution of our photolitographic process (masks, resist..) and by a gradient of the deposition parameters, due to the dimensions of the cathodes and the type of sputtering process employed.

Time stability was estimated by measuring them after a chosen time lapse, from 1 to 36 month. Data for 1, 3, 12, 30 and 36 months have shown both in single junctions and arrays varying from 3×10^{-3} and 2×10^{-2}. All these samples had undergone at least two thermal cycles. The process seems then quite insensitive to aging and cycling.

To conclude, to fabricate reproducible fully non-hysteretic junctions, the best values of Al thickness and oxidation exposure are in the range 40-80 nm and 120-350 Pa·s, respectively. The restriction for Al to the lowest values is due to the need to have smooth interfaces, and, at the same time to keep junction transition temperature as high as possible; in fact while we measured T_c of 8.8-9.0 K for al 30-50 nm, T_c was reduced to less than 8.0 K for Al 70-100 nm. On the contrary, a wider span of the exposure dose is preferable, as it is useful to obtain junctions with different V_c, and possibly some hysteresis of the I-V.

Table 1. Reproducibility Data fir SNIS Josephson Junctions. The Data Reported in the Table are Relative to Devices Fabricated with Two Different Sputtering Systems, HV rf Sputtering and UHV DC Sputtering, the Parameter Homogeneity Resulting therefore Independent of the Machine and Process. Similar Data of Reproducibility have been Obtained, on Fewer Samples, for Aluminum Thicknesses of 40 and 60 nm

	V_c (mV)	I_c (mA)	Comment
wafer-to wafer	0.55 ± 14.5 %		29 devices on 11 wafers
on-wafer	0.51 ± 9.5 % wafer SNS14 [(a)] 0.63 ± 4 % wafer SNIS32 [(b)]	5.5 ± 5-10% [(c)]	8 and 10 devices on each wafer, from 0.2 to 1 cm apart.
notes	(a) 6 data on 1 square cm area (b) 6 arrays and sub-arrays 0.5-1 cm apart	(c) the variance is referred to the appropriate mean, that is to the average of the measured series arrays of 100, 200, 400 and 1600 junctions	For all devices JJ area: 5 μm x 5 μm

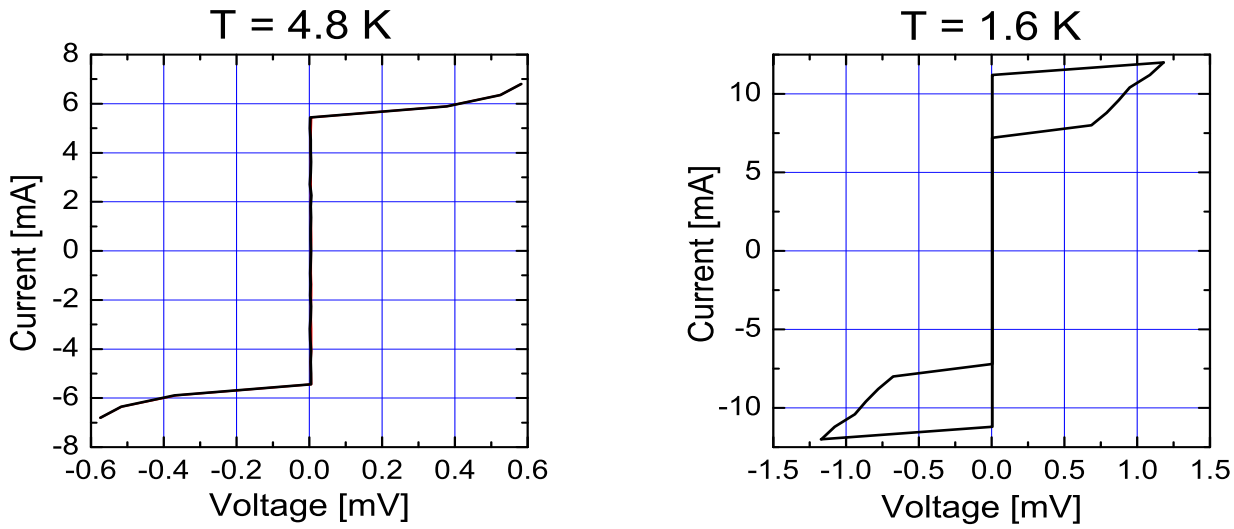

Fig. (5). IV characteristic of Nb/Al-AlOx/Nb overdamped junction without microwave irradiation at different temperatures.

Measurement of the Ic(T) dependence of these junctions from 2 K to 9 K, has shown different behavior as function of the aluminum film thickness. In fact for Al < 50 nm the Ic(T) is similar to SIS Ambegaokar Baratoff dependence, while proximity effect related to the increasing of aluminum to niobium thickness, modify the Ic(T) for Al 50 ≥ nm. In that case three distinct ranges are observed: 1) around 4.2 K the junctions behavior is dominated by the thick Al normal layer, and data are similar to those obtained for junctions with the same electrode thickness and configuration (see ref. [32]). The IV characteristic is hysteretic or non-hysteretic depending on the oxide exposure. 2) Below 4.2 K the junctions eventually become SS'IS, since aluminum is superconductor at 1.5 K, and in proximity with the base niobium film undergoes a N/S transition at a temperature intermediate between 1.5 and 4.2 K. The current increases by a factor of 2, with respect to the value at 4.2 K and the junctions IV characteristic becomes hysteretic, since β_c is now > 1. 3) Above 4.2 K the junctions current decreases, see below, and the behaviour is SNS like, up to the transition, since β_c is now < 1. Fig. (**5**) show the IV characteristic of these junctions at two different temperatures. The temperature dependence of and has shown that higher values of and are obtained at temperatures below 4.2 K, and, what is more interesting, reasonable values are still found at temperatures above 4.2 K.

3.3. Applications to Voltage Standard

Nb/Al-AlOx/Nb, can be usefully employed in programmable voltage standard since they have the following advantages with respect to other technologies.

a) High values of both current density and characteristic voltage can be obtained, compared with other types of junctions

b) Aluminum thickness and oxidation dose parameters can be selected to provide values about 150 μV to optimize at 4.2 K for 75 GHz irradiation.

Owing to the high values of critical current density reduction of junction size appear feasible with overdamped Nb/al-AlOx/Nb. A reduction of the array area of a factor 4 at least is predictable. This will help homogeneity of the fabrication process and of the rf power distribution.

A further possibility would be to use junctions with V_c as high as 500 μV and therefore radiating the junctions with microwave signals at frequencies > 100 GHz; this could reduce the number of junctions needed to obtain 10 V output.

Nb/Al-AlOx/Nb overdamped junctions parameters can be set to fabricate junctions showing no hysteresis, with a purely SNS-like behavior, thus are suitable for PJAVS.

RSFQ circuits to drive the Josephson array can be realized with SNIS technology, in this case realizing trilayers with dedicated parameters, i.e. with V_c as high as possible, > 0.5 mV at 4.2 K.

4. OPERATION OF VOLTAGE REFERENCES ABOVE 4.2 K

An interesting issue is in the possibility of operation at temperatures higher than 4.2 K, in view of the substitution of expensive liquid helium refrigeration systems with the compact cryocoolers which can lead the diffusion of voltage standards to the private companies.

This is a challenge of great importance for superconductive circuits and voltage standards apparently not to be solved in a short period by high T_c junctions. At present, large arrays fabricated with higher critical temperature superconductors, like YBCO or the more recent MgB2, are not yet available, since the technology of these junctions do not allow to achieve the required integration level. One big problem of these junctions is the stability in time and with thermal cycling.

The most interesting results sofar have been achieved with YBCO bicrystal shunted junctions, where quantized steps have been measured near 77 K at 28 mV.

Concerning niobium and niobium nitride based junctions, only NbN/TiN/NbN [35] have demonstrated operation at

these temperatures, achieving a sound result such as a 11 bit DAC with 10 and also 20 V output at 10 K.

However, they are sensitive to temperature changes, requiring a stabilization of the cryocooler at 0.1 K level, have a strong demand on dissipated power and require a top-level, costly, fabrication process.

As for niobium based junctions, SINIS junctions even if have different temperature dependence, depending on the multilayer configuration, the most reproducible devices with symmetric barriers have shown values of Ic generally too low at T > 4.2 K [29, 33].

Among SNS, all the pure metallic barrier are not suitable for operation at T above liquid helium, since their V_c is too low. Only MoSi barrier have a different temperature dependence depending on barrier thickness and for instance, show a reduction of of 0.2 at 4.2 K at 7.5 K, which gives a best V_c of 30 μV [43].

Different from these, the NbSi barrier junctions could provide higher values of Ic and V_c at T > 4.2 K, (see ref. [42]). For these junctions the temperature dependence should still be carefully examined, since in this case the almost semiconductive barrier can have a temperature dependent stability.

In this context, Nb/Al-AlOx/Nb overdamped junctions realized at INRiM are also appealing, since they can be operated at temperatures close to Nb transition, between 8 and 9 K.

First measurement of the quantized voltage steps, radiating the junctions with a 75 GHz source, have shown that an optimal working condition can be obtained at such high temperatures, due to the fact that the amplitude of the n = 1 step normalized to the critical current attains its maximum when the microwave drive frequency fd and the junction characteristic frequency fc are nearly equal. fd = fc corresponds also to a condition of minimal power dissipation [22]. The reduction of at temperatures as high as 7 K is then not critical, since it is partly compensated by the optimal fc /fd ratio. In particular, we have measured on a single junction an amplitude of the n=1 step of about 1 mA at T = 8.3 K on a 5 μm size single junction, flat at nV level [52]. This result has been confirmed by preliminary measurements on small series arrays of 10 and 100 junctions, where a step of hundreds of μA has been observed up 7 K, at voltages of 1.4 and 14mV respectively (See Fig. **6**).

This possibility should of course more deeply investigated, by measuring the step amplitude at various temperatures for increasing number of junctions, in order to establish if any reduction of operative margins is produced [51].

The reduction of the working temperature increasing the number of junctions is presently due to a poor thermal exchange between the array and the corning glass substrate1 mm thick, along with the non-optimal coupling between rf signal and the array. Improved results are expected by using thinner silicon substrate and a refined design of microstrip-line structures.

5. CONCLUSIONS

The extension of DC Josephson Voltage standard to AC has led to the development of different type of circuits, according to the specific application.

In section 2 a comparison of different types of overdamped junctions developed for the large circuits needed by the AC extension of Josephson voltage standard has shown advantages and disadvantages of a certain electrode configuation or material. In order to achieve the desired operating conditions, V_c must be fitted to the drive frequency (i.e. 100 - 150 μV for 70 GHz). The requirements for J_c are different: for low J_c the size of the JJ is large, for high J_c (above 100 kA/cm2) the technological efforts increase significantly (sub-μm JJ, connection of the wiring to sub-μm electrodes with high-current capability, improved cooling needed due to self-heating of JJ in highly-integrated series arrays). And these issues must be attained using a tolerable degree of technological effort, also in terms of allowable integration. In fact, in order to have a widespread development in the world laboratories for these circuits, neither the number of junctions should be increased nor the size reduced beyond a certain limit. All together, these issues are not solved by any

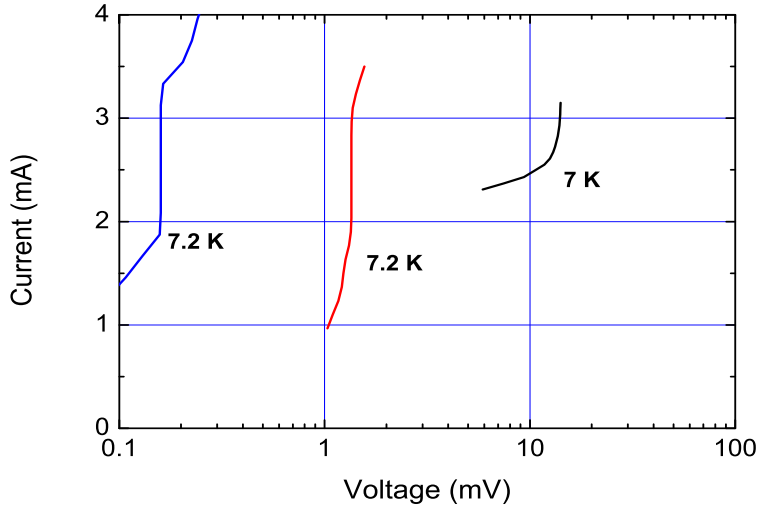

Fig. (6). Quantized steps induced at different voltage levels by a 75 GHz microwave signal are presented at different temperatures. A step 200-300 μA wide is still observed at 7.2 K, while amplitudes around 1 μA are measured at lower temperatures.

of the junctions reported in this analysis, even if some of the described technologies had achieved sound results.

As for SINIS junctions, which has been the most established and successful process in past years, and has been at the basis of both binary array standard at 1V and of PWM and RSFQ circuits, while it allows to use these junctions with microwave drive frequencies of about 75 GHz, thereby reducing their number, it does not allow to obtain adequate values of J_c , therefore requiring a large size. Therefore, no really compact integration of devices is possible while in any case their fabrication process is not trivial, making it difficult to fabricate arrays for voltage up to 10 V and more.

Among SNS junctions, which typically have adequate J_c values, the critical issue is a V_c value sufficiently high. Therefore a huge number of junctions is necessary to achieve quantized voltages with adequate span., even if they are well suited to pulse driven voltage standards.

For this type of standards three possibilities have been mainly addressed:

- submicron junctions such as Nb/HfTi/Nb;
- extremely top-level technology as NbN/TiN/NbN;
- multistacked lumped arrays as Nb/MoSix/Nb and Nb/ NbxSix/Nb.

While each of these three technologies has indeed achieved important results, and it is a good candidate for AC synthesis with enough voltage resolution, all of them require hundreds of thousands of junctions to obtain voltages higher than 1 V and none of them is in any case a good solution for other superconductive electronics circuits, since none of them feature a V_c higher than 200 μV.

Very promising results have been recently reported on NbSi barrier junctions, where by trimming the stoichiometry and the thickness of the barrier V_c and J_c have been varied in a wide range, and the homogeneity of the process has allowed the fabrication of large circuits.

In section 3 results on Nb/Al-AlOx/Nb overdamped SNIS junctions developed at INRiM show the advantages of a really simple technology, which neither requires deep submicron dimensions nor implies the use of extremely large number of junctions, featuring high values of both J_c and V_c. The possibility of realizing junctions with some hysteresis, results also useful for a type of AC standard where pulse modulation is performed by the so-called PWM scheme.

A last major issue of next generation of Voltage standards discussed briefly in section 4 is the possibility of operation above 4.2 K, with considerable advantage for power dissipation.

For this, apart high T_c junctions, still to be improved in reproducibility, only very complex NbN/TiN/NbN juctions have proved to work at temperatures as high as 10 K. The possibility of achieving quantized step of sufficient amplitude (1 mA) also at temperatures as high as 7-8 K in single junctions and something less in 10 and 100 junctions series arrays, on the other hand paves the way to experimental set-up with a simpler refrigeration support also for SNIS junctions based on niobium.

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