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Implementation of PSK Digital Demodulator with Variable Rate Based on FPGA

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Abstract: Aiming at QPSK modulation digital system with variable rate, a novel implementation method based on field programmable gate array (FPGA) is proposed, which can support 4.88Kbps to 2Mbps and even higher continuous bit rate. The design adopts mixed multiplier, numerically controlled oscillator (NCO) and integral comb filter (CIC), and describes the structure of carrier recovery circuit and signal recovery circuit, which can be ported to any FPGA device. The proposed design has its hardware test in the Xilinx Virtex-5 FPGA platform. The hardware test results show that the proposed demodulator only takes up 15% available logical unit of Xilinx Virtex-5 FPGA device, revealing superior ability in efficiency.

Keywords: Bit rate, Field programmable gate array (FPGA), Modulator, Variable rate.

1. INTRODUCTION

With the growing demand for personal communications in the whole world, the using scale of satellite communications has been increasing. Because of its better noise immunity (even at low E_b / N_o, it has a lower bit error rate compared to other methods)and regeneration ability, Phase Shift Keying (PSK) can maintain a high quality of communication service(QoS), which has become the most commonly used digital modulation technique in satellite communication.

In order to meet the users' demands for greater bandwidth of voice, video and data communications, advanced inter-satellite communications must support different rates. The demodulator is a critical part of any air and ground communication receivers, which is used to obtain the needed baseband data from modulated signals. In order to achieve the demodulator with 2Mbps or even higher digital rates, the FPGA can be used to implement variable rate demodulator. The simulation and implementation of current digital demodulators are only for data rate at 2Mbps. However, through rational choice of sampling frequency, higher speeds can be achieved using the current structure of the demodulator.

Literature [1] has proposed a QPSK digital demodulator to complete the demodulation of QAM modulation by adjusting the circuit structure of demodulator; Literature [2] has put forword a digital demodulator without changing the circuit configuration to demodulate QPSK and 8PSK; Document [3] proposed a high-speed digital demodulator with parallel configuration, which can work quickly to achieve QPSK demodulation. However, these all are for fixed-rate, and the rate is lower than 2Mbps.

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The article designs a variable rate QPSK demodulator based on FPGA, and verifies VC707 evaluation board of the Xilinx Virtex 5 FPGA family. The design adopts hybrid multiplier, numerically controlled oscillator (NCO) and integral-comb(CIC), and gives the design structures of carrier and signal recovery circuit. The system may support 4.88Kbps to 2Mbps and even higher continuous bit rate. As a stand-alone design structure, it can be ported to any FGPA platform. Hardware implementation results show that the proposed demodulator only takes 15% of the available logic cells in a Xilinx Virtex-5 FPGA devices, revealing superior efficiency.

2. PRINCIPLE OF PSK COMMUNICAITON SYSTEM

Fig. (**1**) shows the basic schematic of a typical satellite communication PSK system. It contains the source coding of baseband data, carrier phase modulation and AWGN channel(a communication medium between the antenna and the terminal, RF signal transmission model)[4].

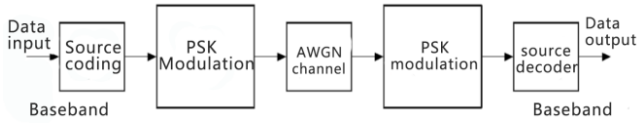

Fig. (1). The basic block diagram of an exemplary PSK communication system.

A reverse process is demanded to obtain the baseband data at the receiving end. The demodulated data can be realized through the regeneration or an analog or digital receiver. The digital implementation of demodulator should prefer to choose the method in literature [5] because digital demodulator is programmable and faster timing recovery compared to analog demodulation.

Table **1** shows the technical parameters of QPSK demodulation. According to the central value in the spectrum of the

modulated signal of the processing inverted image, the sampling frequency is set to 70MHz.

Table 1. Technical parameters of the demodulator.

Index Parameter	Values
IF center frequency	70MHz
ADC sampling frequency	40 Mbps
IF power	-5dBm 到 -20dBm
QPSK modulation	QPSK
Signal mode	continuous signal
Symbol rate	4.88Kbps to 2 Mbps
FEC decoding mode	Viterbi decoding
Phase ambiguity resolution method	by different encoding and decoding methods
Judgment Type	3-bit soft decision

3. PROPOSED DESIGN OF THE DEMODULATOR

Fig. (**2**) shows a block diagram of the digital QPSK demodulator design proposed. It includes three tracking loops: automatic gain circuit (AGC), carrier acquisition/tracking loop and symbol tracking loop.

The tracking and adjustment of AGC loop changes from the variation of input signal power caused by path loss. Carrier tracking loop can eliminate the uncertainty of carrier frequency and phase(due to the instability of the oscillator, the phase elimination in symbol tracking loop, frequency uncertainty of data and the clock synchronization of the receiving data) [6]. A finite state machine is used to select the mode of capture or tracking, and selects and outputs of false lock and solid lock.

4. DESIGN OF NUMERICALLY CONTROLLED OSCILLATOR AND MIXER

The design of a numerically controlled oscillator (NCO) is used to generate sine and cosine carrier [7], binding with the input data after digital modulation. Sinusoidal signals are used as phase components, and cosine signal for generating a quadrature component of a complex signal [8]. Fig. (**3**) shows the design of the structure of NCO. Phase jitter is for obtaining better frequency response. Table **2** shows the technical parameters of NCO.

In the vicinity of the carrier frequency of dependent channel, mixer multiplies digitized input data samples and synthetic carrier, so as to put the needed channel into the

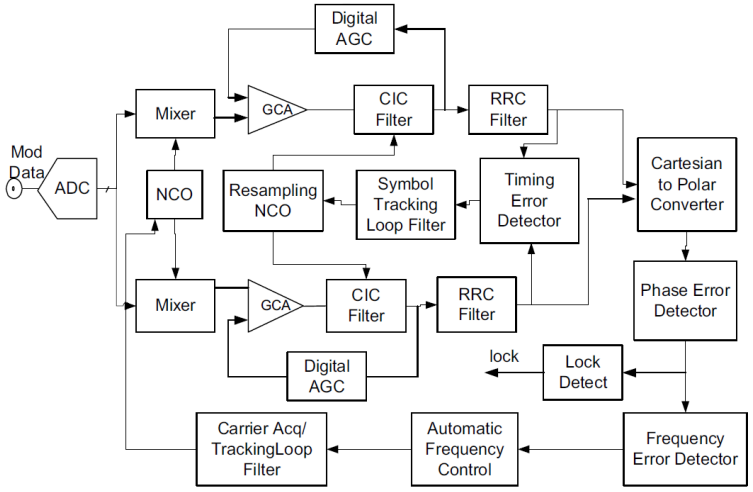

Fig. (2). Proposed structure of digital PSK demodulator.

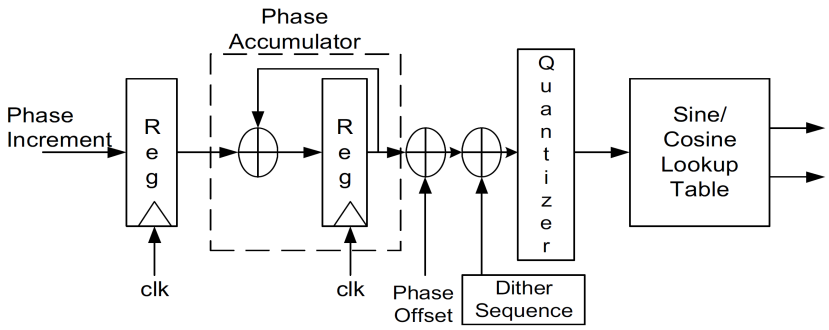

Fig. (3). The design structure of NCO in FPGA.

Table 2. Technical parameters of NCO.

Index Parameter	Values
Sampling frequency	40MHz
Phase increment byte length	32bits
Output bit width	10bits
IQ carrier frequency	10MHz

baseband range. The output of the mixer contains both the and value and difference value of frequency components in the input sampling frequency. In order to verify the design proposed in this article through hardware, the mixer must work under the sampling frequency of ADC in the structure. Table **3** below shows the technical parameters of the mixer.

Table 3. Technical parameters of the mixer.

Index Parameter	Values
Input data bits	10bits
Carrier bit	10bits
ADC sampling frequency	40MHz
Carrier center frequency	10MHz

5. DESIGN OF LOOP FILTER

The loop filter in the demodulator structure proposed is a second order lag filter, as shown in Fig. (**4**). Filter transfer function is:

$$F(z) = C_1 + \frac{C_2}{1 - z^{-1}} \tag{1}$$

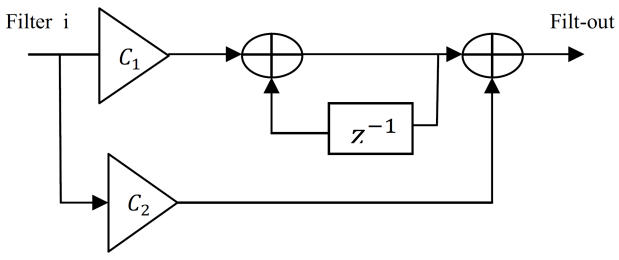

Fig. (4). Digital loop filter.

The bandwidth of second-order phase-locked loop B_n is:

$$B_n = \int_0^{\infty} |H(w)|^2 \, df = \frac{w_n}{2}\left(\xi + \frac{1}{4\xi}\right) \tag{2}$$

According to the loop bandwidth of carrier and symbol tracking loop, loop filter coefficients can be calculated by the following formula:

$$C_1 = \frac{1}{K_o K_d} \frac{8\xi w_n T_{samp}}{4 + 4\xi w_n T_{samp} + (w_n T_{samp})^2}$$
$$C_2 = \frac{1}{K_o K_d} \frac{4(w_n T_{samp})^2}{4 + 4\xi w_n T_{samp} + (w_n T_{samp})^2} \tag{3}$$

In which, w_n is the natural frequency of the loop, T_{samp} is the sampling interval, ξ is the damping coefficient, K_o and K_d are the gain for the NCO and mixer.

6. DESIGN OF CIC AND RRC FILTER

In the proposed structure of the digital demodulator, two functions are needed to further process the signal: low-pass filtering and sampling. Low-pass filtering must be immediate after the mixer in order to eliminate unwanted signal frequency caused by the mixing function. Sampling is to reduce the input sample rate, so as to reduce the process of required release signal to the maximum extent for the subsequent stages [9].

CIC filter is a very efficient method of sampling implementation [10]. Fig. (**5**) shows the structure of the CIC filter, which comprises N cascaded integrators (locked sampling frequency f_s), rate changing factor R, N cascaded comb stages(operating frequency is f_s / R), wherein N is the specific number or the order of filter. CIC filter is an efficient hardware filter structure for performing filtering function with shift register and adder only [5].

The filter has a frequency response function, which is shown below.

$$H_{CIC}(f) = k\left[\frac{\sin(\pi f R)}{\sin(\pi f)}\right]^3 \tag{4}$$

Wherein, f is the normalized frequency relative to the input sampling rate, and k is the filter gain and R is the sampling rate. The pass bandwidth of the filter can be controlled by

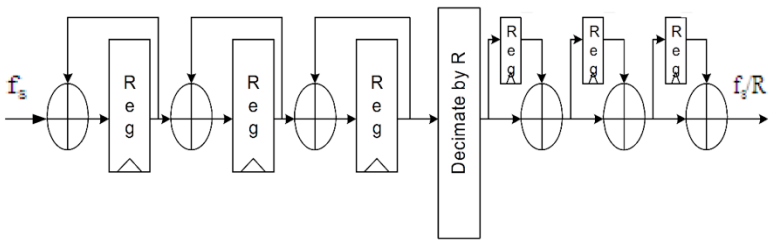

Fig. (5). Structure diagram of CIC sampling filter.

Table 4. Technical Parameters of CIC Filter.

Index Parameter	Values
Input sampling frequency f_s	40Mbps
N	3
Delayed a check points	1
Sampling factor R	3-4096

sampling factors [11], and R can be adjusted to provide a flexible demodulation bandwidth to match symbol boundary. The technical parameters of the filter are shown in Table **4**.

In order to compensate for the band tilt, a programmable finite impulse response filter(PFIR) is used after CIC filter. The accuracy of the density factor can be developed within the range from 1 to 32bits. Figure **6** shows the CIC filter response compensated when the symbol rate is 2Mbps.

In order to increase the signal to noise ratio (SNR) to achieve better signal estimation, the root cosine filter is applied as a matched filter in the demodulator. The amplitude response of raised cosine filter is:

$$H(f)=\begin{cases} T_s & ,|f|\le \dfrac{1-\alpha}{2T_s} \\ T_s\cos^2\left(\dfrac{\pi T_s}{2\alpha}\left(\left|f-\dfrac{1-\alpha}{2T_s}\right|\right)\right) & ,|f|\le \dfrac{1+\alpha}{2T_s} \\ 0 & ,|f|>\dfrac{1+\alpha}{2T_s} \end{cases} \quad (5)$$

In which, T_s indicates the interval of unit symbols, α expresses roll-off factor and is set to 0.35 in the system implementation.

7. EXPERIMENTAL RESULTS AND ANALYSIS

The whole design is realized through Verilog HDL 2001, and without FPGA IP cores, so the proposed design belongs to independent platform that can be applied to any FPGA module such as Xilinx and Actel. Nevertheless, Xilinx-ISE9.2i is used in the FPGA implementation experiment in this paper, and simulation of performance function uses Questa Sim 10.0b which is matched with Xilinx Virtex-5 FPGA. Fig. (**7**) shows the implementation of hardware test system of the proposed design, including COMTECH modem for modulated input, Tektronix TLA5201B logic analyzer for capturing and observing the output of demodulator.

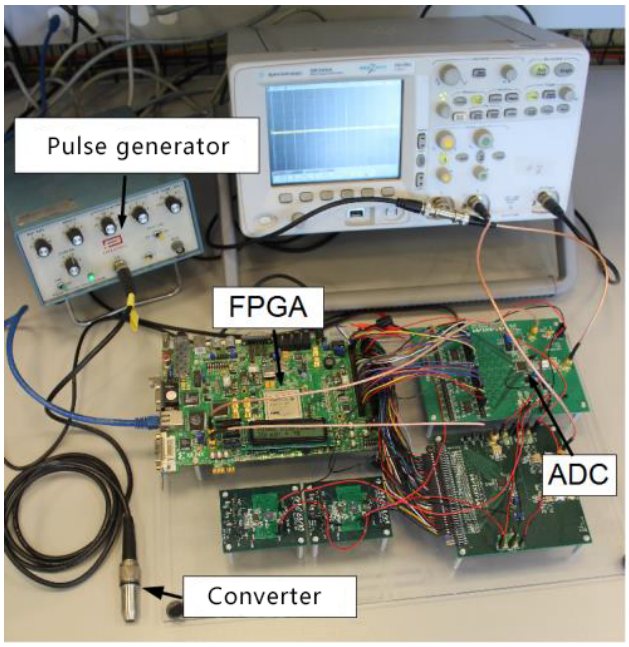

Fig. (7). Diagram of hardware test system.

Simulink models are used to simulate different parameters of the design, making it easier to complete the hardware implementation. Fig. (**8**) shows the phase constellation diagram and eye diagram at port 4 of demodulator when the symbol rate is 2Mbps.

Fig. (**9a**) shows phase error response of carrier tracking loop between the input and the local carrier in the condition of closed loop. Fig. (**9b**) shows the theoretical value and the simulation value of BER when the symbol rate is 2Mbps. PSK coding system reaches the realization margin of 0.5dB and the coding gain is approximately 5dB.

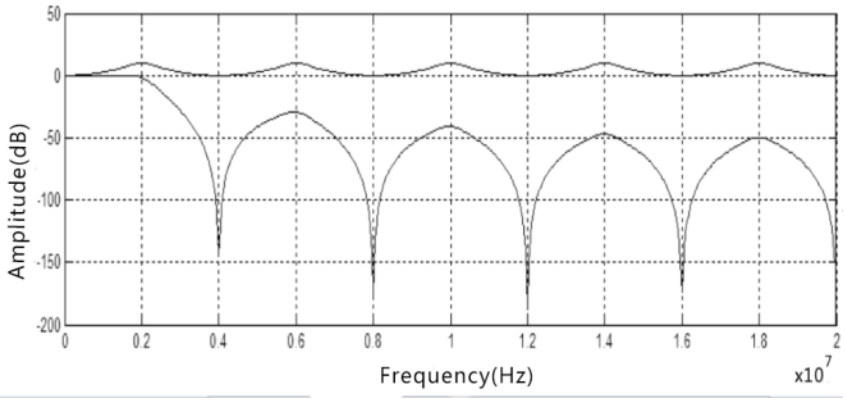

Fig. (6). CIC filter response compensated.

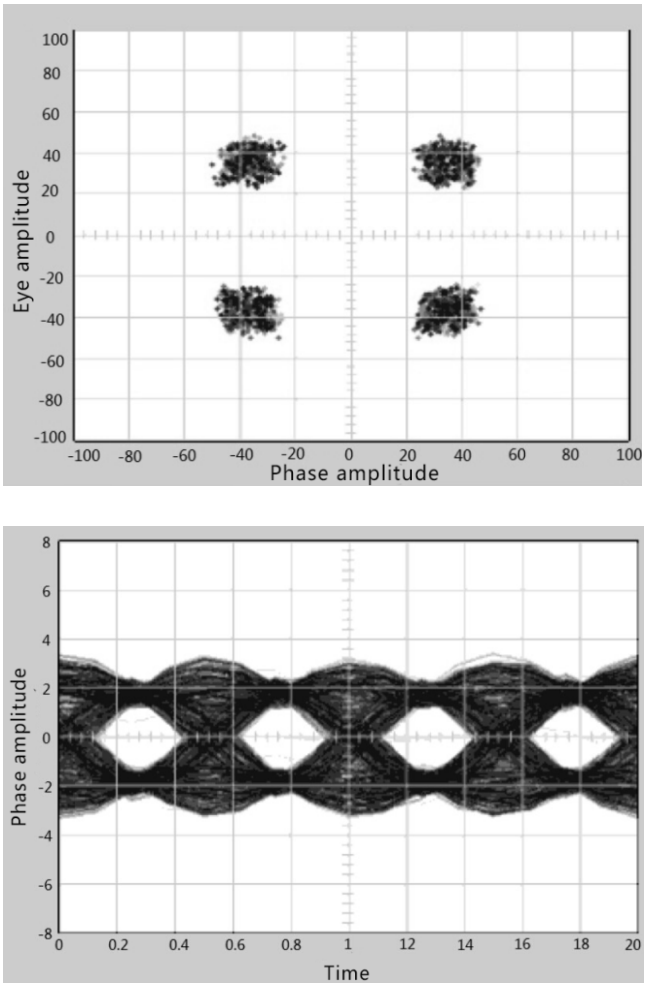

Fig. (8). QPSK constellation and eye diagrams.

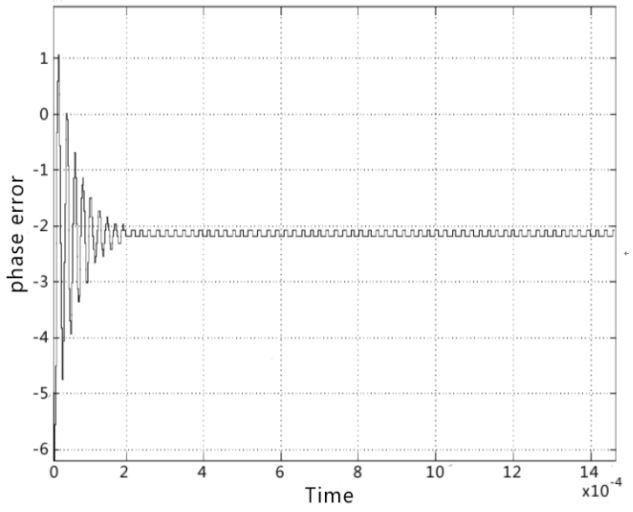

Fig. (9a). Carrier phase error of the locking carrier tracking loop.

Fig. (**10**) shows the FFT plot of 16384 point by 70MHz carrier after ADC and 40Mbps sampling. The spurious-free dynamic range (SFDR) is larger than 50dB, which can be seen in that the performance of demodulator is independently distributed in relation to the ADC dynamic range.

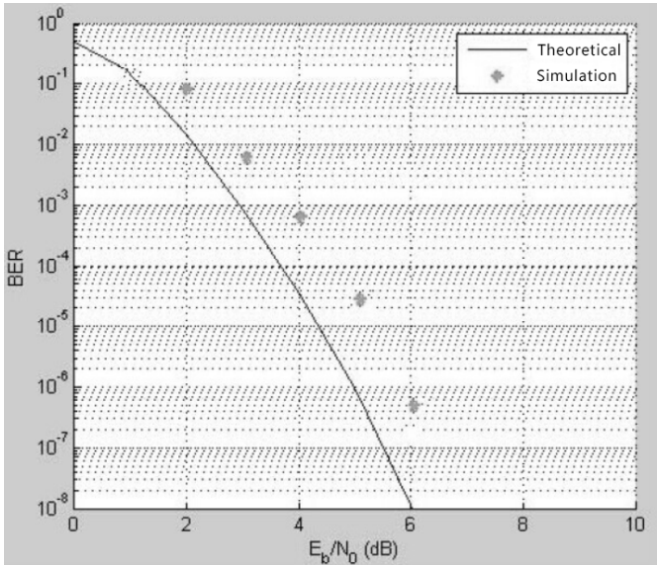

Fig. (9b). BER curves of carrier tracking loop.

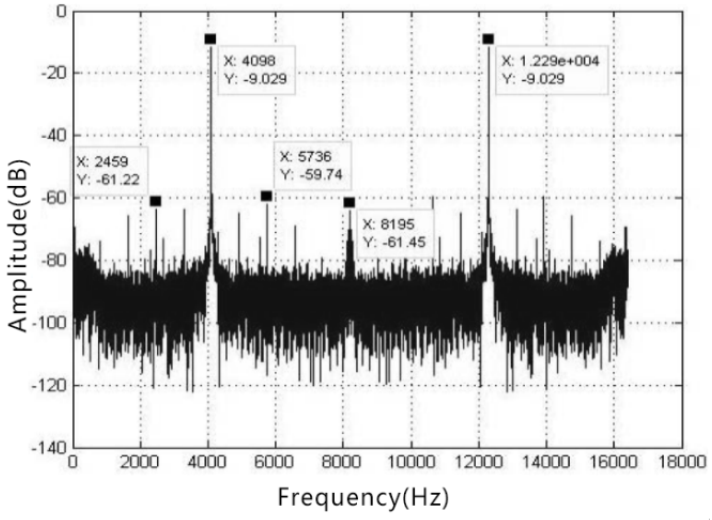

Fig. (10). FFT plot with ADC characteristics.

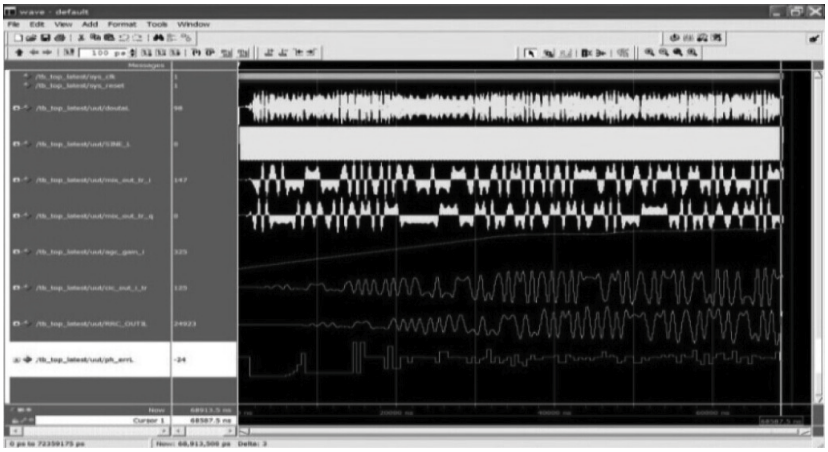

Fig. (11). Functional simulation results of digital demodulator.

Modulated signal should go through the ACD Analog Devices AD9054A integrated by Xilinx development board, and capture its output by the logic analyzer. The data is stored in the ROM of FPGA, and used as the simulation input of the entire design. The result of Questa Sim 10.0b is shown in Fig. (**11**), which shows the output signal at different stages of the digital demodulator. The simulation results include modulated signal input when phase-error is in locked state, combined carrier of NCO, output of mixer, output of digital ADC and output of CIC filter.

CONCLUSION

This paper presents a hardware efficient QPSK digital demodulator structure. The design uses a programmable data rate, which is applicable to advanced satellite communication system. Proposed hardware architecture occupies only 15% of the overall chip resources of Xilinx Virtex-5 FPGA hardware platform, and the presented design is platform-independent, which can be transplanted at any targeted FPGA.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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Declared none.

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