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Development of Automotive Collision Avoidance System Based on Intelligent Control

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Abstract: With the development of automotive industry, the traffic accident caused by automotive collision has become a social problem in the world. Aiming at improving the safety of automotives and reducing the collision accidents, an automotive collision avoidance system based on intelligence control is researched. As the control core, a 16-bit microcontroller receives the distance signal of the front car from ultrasonic distance measuring module, and controls a motor to realize the speed control of the vehicle. An infrared sensor is used to measure the car speed, and this signal is sent to the microcontroller to make the motor control more precise and stable. A small motor is installed at the car throttle, and the microcontroller controls this motor to adjust the opening of the throttle, thus avoiding human operator errors that the traditional mechanical throttle makes. The main modules of this intelligent control system have been developed; these modules include the PWM module, ECT module, PIT module, and PLL module. The intelligent throttle has been studied. The result shows that the system is reliable and has high-resolution control accuracy.

Keyword: Automotive collision avoidance, intelligent control, ultrasonic signal infrared sensor, speed control.

INTRODUCTION

According to the Ministry of State Security of PRC, China State Security Bureau, 110000 people lose their lives because of traffic accidents in China each year, making China become one of the world leaders in terms of traffic accident-related deaths. Data was taken from the Transportation and Communities year book of China that road traffic death rate was increased by 95 percent from 1985 to 2005 (Barboza, 2011). How could this happen? What are the main causes of this and what could Chinese people do towards this? First here are two traffic accidents in China and the USA [1].

The form of road traffic safety is very grim in China. Statistics shows that the number of fatal traffic accidents in China of each year is nearly 100000, accounting for one point five percent of the total death toll. The seventh cause of death. The minutes died in under the wheel. Every minute, a person become disability because of traffic accidents. Each year, the economic losses caused by traffic accidents reach hundreds of billions.

In recent years, along with the increasing of all kinds of vehicles, traffic accidents continue to occur. According to relevant statistics, China has 1.9% of the world's automobile, and accounts for15% of the traffic accidents of the world, each year, the number killed in traffic accidents is more than 100000, in which is the highest in the world. Traffic accidents continue to occur, caused a great threat to people's life and property safety and social order and stability, and has become a serious social problem.

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Therefore, the safe driving cars will become one of the main causes for the stability of the family, The incidents in the real life have occurred when the car rear-end, he mistakenly stepped on the accelerator instead of the brake causing a fatal car crash and this tragedy event deeply touched my heart. With the development of the microcontroller's electronic technology, you can make the car become more intelligent [2]. In China, most of vehicles are equipped with airbags and seat belts. However they are just Passive safety device, whose safety factor is not high. Aiming at enhance enhancing the positive safety of the vehicle, an intelligent collision avoidance system is developed. This system can detect the distance betweenfrom the front car distance and control the car speed automatically to avoid collision. The research is developed with low-cost, high performance, small footprint, high safety factor, market prospects, and it is with greater significance to promote

China's actual level of the automotive industry. The system is characterized by the integration of software and hardware, low cost, high performance, small package, and high safety factor, which make it promising in the future market [5].

THE OVERALL BLOCK DIAGRAM OF THE SOFTWARE

The overall block diagram of software design is as shown in Fig. (**1**):

The core of this program is based on MC9S12xs128. When the ultrasonic signal triggers the interruption routine, the DC motor would be controlled accordingly.

Program flow chart as shown in Fig. (**2**):

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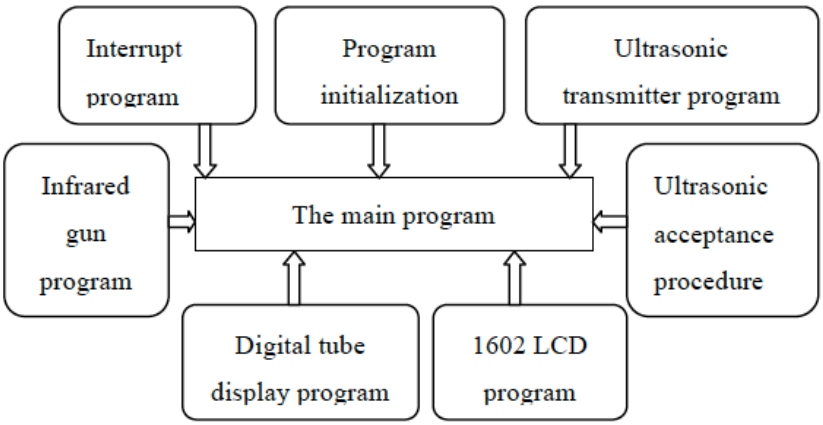

Fig. (1). Software design diagram.

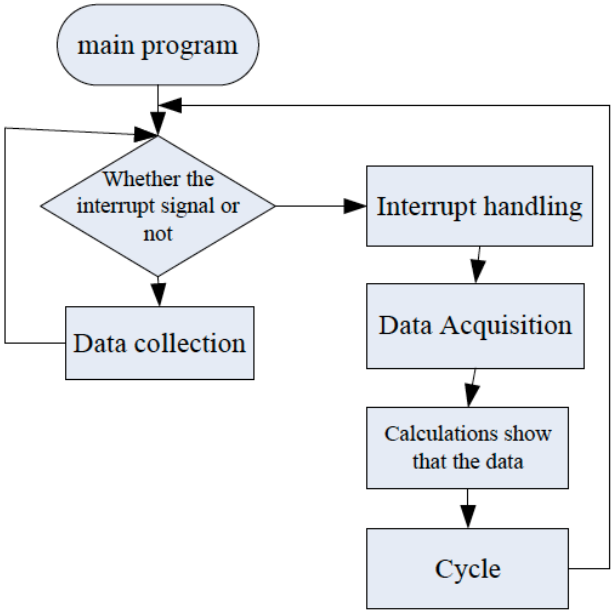

Fig. (2). Software design flow.

PWM MODULE PROGRAM

The PWM has eight output channels, and each output channel can be independently output. Each output channel has a precise counter (calculated for calculatinges the pulse number), a cycle of control registers and two alternative clock sources.

Each PWM output channel can modulate the waveform with the duty cycle range from 0 to 100% [7].

The Main Features of the PWM

The PWM has eight independent output channels, and each output channel has a precise counter; PWM output enables each channel to be controlled by programming;

The flip control for PWM output waveform can be achieved by programming; the cycle and pulse width can be double-buffered [3].

When the channel is turned off or PWM counter is 0, it can only work by changing the cycle and pulse width; 8 bytes or 16 bytes of channel protocol; there are four clock source options (A, SA, B, SB), which provide a wide range of frequencies [8].

Related Calculations

1) Calculate the clock

The clock SA is generated by PWMSCLA register settings to the A clock frequency.

Clock SA=Clock A/(2*PWMSCLA);

The clock SB is generated by PWMSCLB register settings to B clock frequency.

Clock SB = Clock B / (2*PWMSCLB);

2) Period calculation

①When CAEx=0, that was left linear output:

PWMx cycle=channel clock cycle * PWMPERx;

②When CAEx=1, namely, the center-aligned output: PWMx cycle=channel clock cycle*(2* PWMPERx);

3) Calculation of duty

When PPOL=0: Duty=[(PWMPERx-PWMDTYx)/PWMPERx]*100%;

When PPOL=1:

Duty=(PWMDTYx/ PWMPERx)*100% ;

PWM Initialization Procedure

```
PWME_PWME2=0x00; // Disable PWM
PWMPRCLK=0x33; // 0011 0011 A=B=24M/8=3M
PWMSCLA=150;  // SA=A/2/150=10k
WMSCLB=15;   // SB=B/2/15 =100k
PWMCLK_PCLK2=1; // PWM3-----SB
PWMPOL_PPOL2=1; // Duty=High Time
PWMCAE_CAE2=0; // Left-aligned
PWMCTL=0x00; // no concatenation
PWMPER2=100; // Frequency=SB/100=1K
PPWMDTY2=0;  // Duty cycle = duty
PWME_PWME2=1; // Enable PWM
```

ECT MODULE PROGRAM

ECT Feature

The ETC has four IC channels, and it can set 16 holding registers for buffering to capture the results; has four 8 pulse accumulators, four 8 holding registers associated with the buffer IC Channel; four eight-channel pulse accumulators can be cascaded, form two 16 pulse accumulators; four scaler 16 modulo counter is decremented; four optional delay counter is used to enhance the anti-jamming capability; only supports 16 access in IP bus.

ECT Operating Mode

Stop: Since the clock is stopped, timers and counters are closed; freeze: timers and counters are kept running until TSFRZ bit of TSCR ($06) is set to 1; wait: Counter keeps running until TSWAI bit of TSCR ($06) is set 1; normal: timers and counters are kept running until TEN-bit of TSCR ($06) and MCEN bit of MCCTL ($26) is cleared respectively.

ECT Composition and Mode of Operation

Two pairs of 8 bite pulse accumulator can also be cascaded to form a 16-bit pulse accumulator PACA, PACB. 16 decreasing modulus counter (MDC) is the additional ECT, it is not only a functional timer with independent programmable scaler, auto-reload and interrupt capability, but also provided transmission timing control signal for the IC, PAI register to keep registers. Whenever the MDC back to 0, the ETC controlled IC and PAI rigister's content to the respective buffer register in a given period of time. Of course, MDC is also used as an independent clock reference with timer interrupt function [6].

Operational State of Timer and A/D Counter

Stop (STOP): Because PCLK and ECLK have stopped, timer and A/D counter closed;

Debug mode (BDM): As long as it does not meet TSBCK=1, timer keeps running;

Interrupt wait (WAIT): As long as it does not meet TSWAI=1, counter keeps running;

Normal (Normal): As long as it does not meet TEN=0 and MCEN (MCCTL in)=0, the timer keeps running;

Ban (TEN=0): timers and MDC stop,

ECLK/64 clock is disabled;

Ban (PAEN=0): The operation of all pulse accumulators is stopped, but the register can be accessed;

MCEN: 0: modulo counter is stopped;

PAEN: 1, 16-bit pulse accumulator is activated PAEN: 0, 8-bit pulse accumulator 3 and 2 can be activated;

PBEN: 1, 16-bit pulse accumulator B can be activated;

PBEN: 0, 8-bit pulse accumulator 1 and 0 can be activated [4].

ECT Initialization Procedure

```
TIOS=0xFE; // Set input capture channel to PT0
TCTL4=TCTL4_EDG0A_MASK|TCTL4_EDG0B_MASK; // PT0 capture rising edge and falling edge
TSCR2=0x87; // Timer overflow interrupt enable, divided by 128
TIE=0x01; // Open PT0 interrupt
TSCR1=TSCR1_TEN_MASK; // Timer Enable
```

PIT MODULE PROGRAM

PIT is a 24 timer array, and the peripheral modules can be used to trigger or cause periodic interrupt. Two microtimers are 8-bit micro Timer0 and micro timer1; four is 16-bit timers Timer0, Timer1, Timer2, Timer3.

Four kinds of operation modes: run mode, basic modes of operation; wait mode, PIT mode of operation by PITSWAI of PITCFLMT register control; stop mode, which has the full stop or pseudo stop mode, PIT stop running; freeze mode, PIT mode of operation by PITFRZ of PITCFLMT register control.

PIT Features

When 16-bit and 8-bit counters are reduced to 0, PITLD register is reloaded, and the corresponding timeout flag the PTF bit of PITTF is set to 1. Timeout period is a function of the PITLD, PITMTLD and fBUS.

Time-out period=（PITMTLD+1）*(PITLD+1)/fBUS;

40MHz bus clock, the maximum timing period is equal to（255+1）*（65535+1）/25ns = 419.43ms.

PIT Interrupt Interface

Every timeout event can trigger an interrupt request, which has a separate PINTE bit to achieve this function for each timing channel. When PITNTE is set 1, appropriate PTF of PITTF timeout flag bit is set to 1, and it will request an interrupt service. PTF can be cleared by writing a_1 to the corresponding bit manually.

PIT Hardware Trigger

PIT module contains four hardware trigger signals in PITTRIG [3:0], and each timing channel has one. These signals can be connected to Soc module and is used to control peripheral devices, such as cycle ATD

conversion; whenever a timing channel arrives, the corresponding PTF bit is set to 1, and the trigger signal PITTRIG triggers a rising edge.

PIT Initialization and Shutdown

The PITE bit is set to 1 before initializing all registers, and the registers may be written in any order before PITE is set. When PITCE, PITINTE, PITE is cleared, the corresponding PIT interrupt flag bit is cleared. Suppose there is a queue of PIT interrupt requests, a spurious interrupt may be generated. There are two strategies to avoid this spurious interrupt:

1) Only in the ISR (interrupt service routine) Reset PIT interrupt flag when entering the ISR, CCR in the I mask flag is set automatically. I mask flag should not be cleared before the PIT interrupt flag.

2) After I mask is set using SEI instruction, PIT interrupt flag can be cleared. Then use the CLI command to re-enable interrupts.

A flag can be cleared by writing 1. If you want to store instructions or directives,write 1 in the determined position (STRORE and MOVE), do not use the BSET instruction, as any C language statements may be compiled into BSET instruction. "BSET flag_register, #mask", can not be used to clear the flag, because BSET is readable, writable and it can modify instruction. BSET instruction can operate or operator the value of flag_register and mask bit after the or operator values return, BSET will be cleared all flags before the set.

PIT Initialization Procedure

```
PITCFLMT = 0x00; //close PIT
PITCE = PITCE_PCE0_MASK;
// Open the timer channel 0
PITMUX = 0x00;
//Timing channel 0 using micro counter 0
PITINTE = PITINTE_PINTE0_MASK;
// Enable timing channel 0
PITMTLD0 = 80-1; // Set micro counter load register 0
PITLD0 = 1000-1; // Set 16-bit counter load register
PITCFLMT = PITCFLMT_PITE_MASK; // Enable PIT
```

PLL MODULE PROGRAM

PLL: Phase synchronization logic. The closed loop is an automatic frequency (phase) adjustment process, so called ring. Phase-locked loop is composed of analog phase-locked loop and digital phase-lockedloop.

Phase-locked loop line was originally used to improve the television receiver and frame synchronization to improve the anti-jamming capability. In electronic instrumentation, Phase-locked loop plays an important role in PLL frequency synthesizer, phase meter and other equipments. PLL applications currently focus on the following three aspects: firstly, signal modulation and demodulation; secondly, frequency modulation and demodulation; thirdly, signal frequency synthesizer circuit.

Analog Phase-Locked Loop and Digital Phase-Locked Loop

The analog phase-locked loop consists mainly of extraction circuit, voltage controlled oscillators, phase by phase comparator reference and the control circuit etc. The voltage controlled oscillator outputs equal amplitude signals which are very close to the needed frequency, then simultaneously fed these signals to the phase comparator together with a reference signal extracted by the phase reference extraction circuit from signals. The error formed by comparison is used to produce continuous change of voltage controlled oscillator frequency along a direction of reduced absolute error through control of circuit, to achieve phase lock and reach synchronization. The output signal frequency of the divider is very close to the desired frequency, compared with the signal phase of the reference signals in a phase comparator simultaneously. The comparing results indicate when the local frequency is higher, it is necessary to erase one pulse of input frequency divider via complement wipe gate, which equals to a decreased local oscillation frequency; on the contrary, if the local frequency is lower, it is necessary to insert one pulse between two input pulses of input terminal of pulse divider, which equals to an increased local oscillation frequency, so as to achieve synchronization.

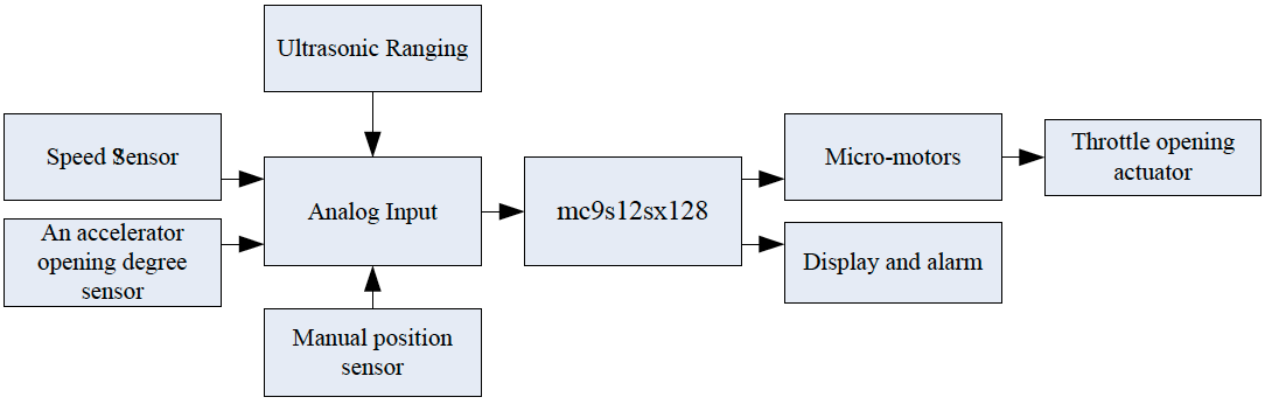

Fig. (3). Intelligent electronic throttle schematics.

PLL Initialization Procedure

```
CLKSEL=0X00;
PLLCTL_PLLON=1;// OPEN PLL
SYNR=0xc0 | 0x09;
 // VCOFRQ[7:6];SYNDIV[5:0]
 // fVCO= 2*fOSC*(SYNDIV + 1)/(REFDIV + 1)
 // fPLL= fVCO/(2*POSTDIV)
 // fBUS= fPLL/2
 // VCOCLK Frequency Ranges VCOFRQ[7:6]
REFDV=0x80 | 0x01;
 // REFFRQ[7:6];REFDIV[5:0]
  POSTDIV=0x00;
   asm(nop);
  _asm(nop);
  while(!(CRGFLG_LOCK==1));
  CLKSEL_PLLSEL =1;
```

INTELLIGENT THROTTLE CIRCUIT

Traditional electronic throttle controls are based on the judgment of the human brain, which is uncertain sometimes, thus the throttle opening is unstable, which results in excessive oil consumption than the smart throttle (fuel ratio constant).

It's obvious for the electronic throttle that the wiring harness can be used in place of cable or lever, and a mini motor is mounted near the throttle to adjust the opening of throttle. The so-called "line drive", is to replace the original mechanical transmission mechanism. That intelligent Electronic throttle transmits the desired throttle opening signal to MC9S12xs128 by adjusting the position sensor with hand, through the analysis of the obtained data (torque and speed), the signal will be output to drive the motor to adjust the opening degree of the oil valve. Thus the engine is always in the best condition, which improves the vehicle performance, enhances driving comfort, reduces fuel consumption, reduces emission and better to meet the requirement of environmental regulations [9, 10].

CONCLUSION

The research uses ultrasonic distance measurement principle and a safe judgment function is developed. When the distance between the car and the obstacle is less than a setting safe distance, the system can alarm, and with the continuously shrinking closer, it is possible to gradually slow down. This technology is a great innovation of modern vehicles for automotive safety and energy produce with more far-reaching significance.

In this research, the ultrasonic distance measurement principle is used, and a safe judgment function is developed. When the front car distance is less than a preset threshold, the system begin to alarm the driver, and automatically decrease the car speed in an intelligent way when the front car distance is shorter. This technology will have an important effect on the safety and energy saving for automotive driving.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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