Design of a Programmable USB I/O Main-Board with Development Features

Mazin M. Al Hadidi*[,1], Yasir Khalil Ibrahim[2] and Yarob Istitieh[2]

[1]*Department of Computer Engineering, Al-Balq'a Applied University, Jordan*

[2]*Department of Computer Science, Jerash Private University, Jordan*

Abstract: The strategy this work follows as to achieve its goal, is to put a very first stone in the way of making a USB peripheral. This is done by developing a USB I/O main-board that features some properties usually known of development board; however, this main-board is best identified as an I/O board as it remains in the final product (i.e. it is employed by the final USB peripheral), this identification, called the main-board's description.

The main-board developed as a moderate number of sub-circuits that achieve several functions, the choice of connectors used to plug LEDs, switches and daughterboard.

Keywords: USB, I/O main board, daughter board, module, programmable board.

MAIN-BOARD'S DESCRIPTION

The main difference between development boards and I/O Modules is the simple fact that they are boards and modules, respectively. This can be translated into the fact that I/O modules are designed to remain as a final product, while development boards will only help someone to work out a good design, but once the design is ready for production; the role of the development board will be over. A consequence of this is that in the former case, a number of I/O modules equal to the number of products released will be needed, whereas in the latter case, the number of development boards is completely independent from the amount of production, and is frequently one. Because of the purpose of each, development boards will tend to be main-boards (being ready peripherals stuffed with development features and I/O capabilities). While I/O modules will mostly be daughterboard's; however, this is not a valid distinguishing criterion as it consequently follows from another more essential quality, next to it being dependant on the complexity and requirements of each type of products.

The main-board of this work is thus an I/O module, rather than a development board, as it has intended to be incorporated in the final product. However, the main-board of this work is pretty different from ordinary I/O modules, which contributes into making it a rather-unique product. The main characteristics of this main-board that differentiate it from ordinary I/O modules, which are utilized to gradually develop a satisfying description of this main-board, are the following:

1. It's programmable, though most I/O modules aren't, as this usually won't support the simplicity objective of an I/O module. It's thus a programmable USB I/O module.
2. It's a main-board to which [simple] function daughterboard's are attached, rather than being a [simple] daughterboard that attaches to peripheral main-boards. This is a consequence of the design's objective of letting the I/O module handle most of the complexity, as to allow for a very simple daughterboard, this is the real reason of enabling programmability. It's thus a programmable USB I/O main-board.
3. It has some development features, those are, the availability of a power switch, reset switch. It has dedicated pins used to connect front-panel switches and LEDs that controlled by the microcontroller's program (the firmware). It also has a programming framework and advised debugging ROM monitoring system. It is thus a programmable USE I/O main-board with development features.

Sub-Circuits

This section deals with sub circuits used in this design and gives a brief description of each one. Sub circuits entitled with "TA" "Typical Application” are those advised by different manufacturers, others designed through the work course.

1. Basic Microcontroller's Support: offers the mandatory support needed by the microcontroller chip to launch and execute instructions, usually advised by the manufacturer (Except for the power sub-circuit, which is a shared resource that is designed to satisfy the power requirements of the whole board).

- The Power sub-circuit.
- [TA] The Power Connections of the Microcontroller.
- [TA] The Crystal Connections of the Microcontroller.
- [TA] The PLL Filter Sub-circuit of the Microcontroller.
- [TA] The USB Pad Connections of the Microcontroller.

*Address correspondence to this author at the Department of Computer Engineering, Al-Balq'a Applied University, Jordan;
E-mail: trueamman@yahoo.com

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1.1. The Power Sub-Circuit: The first design decision to consider in the case of the power sub-circuit is whether the main-board should be bus-powered or simply self-powered, using simple outlet linear transformer with a linear regulator on-board as to eliminate the 60Hz ripple. As most design decisions of this main-board will be considered in the light of the already-developed description of the main board, we believe that a programmable I/O main-board, for which flexibility is a major requirement, it's very desired that the main-board offers the maximum flexibility for the designer, as to go on with his favorite powering strategy. When someone considers this, it will be clear that using bus-power to power the main-board, someone will be able either to keep on using the amount of bus-power left as to fulfill his daughterboard power requirements, or might use an external supply, consuming as much power as needed. This simple (though effective) approach however will not enable someone to mark his peripheral as" self-power " in the USB descriptors as a small amount of bus power will always be needed to operate the main-board circuitry, this isn't considered to be a real limitation as long as the amount of bus-power consumed by the main-board is not much. A lot of unnecessary complication is required if someone was to implement true selection between self-power and bus-power that will influence the whole system; the main-board and daughter-board(s), which is believed not to be necessary.

The AT89C5131A-M (microcontroller) has a low power supply range from 3 to 3.6V, rather than an extended range from 3.3 to 5.5V when the embedded USB function is used. This has the negative impact on the system of requiring a voltage regulator sub-circuit, as the USB bus voltage $\mathbf{V_{BUS}}$ will vary between 4.4(or 4.75) and 5.25V [1] depending on the host (or hub) being of the high-power type or the low-power type discussed in the USB specifications document. Low-power upstream hosts (or hubs) might be power-limited hosts relying on batteries as a mere source of energy (laptops, handheld PDAs) or a hub of the bus-powered type (most hubs usually seen are self-powered).

The voltage-regulator sub-circuit thus must be able to accommodate this variance, and provide a sufficient current to run the microcontroller chip and any other component that requires a regulated voltage. According to [2], the supply current consumed by the AT89C5131A-M chip is at least 17.8mA with an oscillator frequency of 32MHz, assuming that the chip is driven from an external oscillator (the internal oscillator is turned off) and all the ports are detached, which obviously makes a very ideal test environments for which the measurements aren't expected to be realistic, this consumption is claimed to be only "slightly" increased when the internal oscillator is used [2].

Considering the case of our bus-powered main-board, where the bus power current is already constrained by an upper limit of half an ampere (100mA is allowed once attached, then it can be configured *via* the descriptors to consumption of up to 500mA), it might be a good idea to use a regulation sub-circuit that's able to provide that much of current, since most through-hole three-terminal regulator are pretty generous in that regard (3A typical), this arrangement will have the following advantages:

1. This way, the USB main-board will be able to offer full-bus-power access to the regulated voltage for all the sub-circuits of the system. Using the extended supply range variant AT89C5131A-M however, this would not have been possible using its advantageous extended power supply range. Neglecting the dirty-probably unsuccessful, method of using the V_{REF} USB D+ pull-up signal as a source of power, as it's merely intended to enable programmable detachment from the USB bus. This pull-up voltage V_{REF} is defined in the specifications [1, 3] to be in the range of 3.6V, which is given by an internal regulator in the case of the extended supply range variant; the AT89C5131A-M.

2. Furthermore, this will make a good idea of passing the regulated voltage to daughterboard(s) *via* the defined interface, along with the unregulated. Bus power voltage $V_{BUS,}$ as this will support the major design objectives of increased flexibility and simple function daughterboard(s), where daughterboard(s) are free to use the unregulated voltage (4.4 to 5.25V worst case), the regulated one (to be selected in the range 3.0 to 3.6V), or another external source of energy.

1.1.1. Adjustable Three-Terminal Regulators: Those offer the simplicity of a three-terminal regulator with the flexibility to achieve a non-standard voltage level, or a one that you can't easily find, like in the case here where a voltage level ranging from 3 to 3.6V required.

Adjustable three-terminal regulators are different from the original three- terminal regulators in the aspect that they are fixed to a band-gap voltage of 1.25V, with the ground terminal called the adjustment terminal and intended to be raised above ground using a voltage divider network as a achieve any multiplication constant that is higher than one.

The regulated voltage uses a feedback network to multiply the band-gap reference voltage by any factor. For example, if we ensured a band-gap voltage of 1.25V across half the output regulated voltage, we achieve a regulated voltage of 2(1.25) ≈ 2.5V, assuming conformance to the minimum allowed drop out $\mathbf{V}_{OUT} - \mathbf{V}_{IN}$ for one adjustable regulator, which equals V for the original yet - popular LM317.

In our sub-circuit here, we wouldn't tolerate the 3V minimum dropout of a classical three-terminal regulator, like the LM317, as the USB power voltage $\mathbf{V}_{BUS}$ will have a worst-case range of 4.4 to 5.25V (with a low-power upstream host/hub), which dictates a minimum allowed dropout $\mathbf{V}_{OUT} - \mathbf{V}_{IN}$ of less than (or equal to) $\mathbf{V}_{BUS\ (MIN)} - \mathbf{V}_{REGULATED}$ where $\mathbf{V}_{REGULATED}$ is to be chosen in the range of 3 to 3.6V, giving arrange for minimum allowed dropouts of 0.8 to 1.4V for a chosen adjustable liner regulator. A maximum dropout voltage of 0.8V (800mV) is needed as to achieve a 3.6V linear regulation, this value however won't be found in classical adjustable regulators, that is, someone will have to search for a low-dropout or a very low-dropout regulator.

Taking 3.3V as a chosen regulated voltage level, the maximum allowed dropout of a chosen adjustable regulator will be 1.1V, which is a moderate value that might be more easily found. We might instead choose a regulated voltage of 3.0V to further increase compatibility and worst-case conformance, but this will most probably be an exaggeration, as the 3.3V voltage level is an appealing one (compatible with most CMOS technologies, in the mid-point of the low supply range of the chip, making room for larger drops, etc.), furthermore, the 4.4V minimum is an exaggerated minimum of the USB supply voltage that will most probably be achieved in very special condition (of low-power upstream hosts /hubs with the system overloaded), in which case we will have to tolerate an out-of-regulation under-voltage condition of 3.1 or 3.2V, which is perfectly acceptable in our case.

This sub – circuit is very straightforward to analyze, ensuring a band – gap reference voltage of V_{REF} across R1 ÷ R2 of the output voltage, we have an output voltage approximately equal to (R1 + R2) ÷ R1 × V_{REF} ≡ (1 + R2 ÷ R1) × V_{REF}. NOT that this analyses assumes that the ADJ terminal doesn't sink nor supplies current, assuming that it supplies an amount of current equal to I_{ADJ} however, someone can easily see using the superposition principle applicable in linear networks that the voltage will be increased by the amount I_{ADJ} × R2, as this ADJ current will pass through R2 to ground, resulting in the expression show below this typical application schematic.

Note that however, a the ADJ pin current will range between 60μ and 120μ amperes, a much better approach instead of inserting I_{ADJ} into the equation, is that we design a voltage divider that's stiff enough with respect to the maximum ADJ pin current, which can be explained in terms of either input /output impedances or input /output currents. However, the specified parameter in this case is the supply current of the ADJ pin, this case is much better handled with the currents terminology. As to form a stiff voltage divider, which means a divider whose division ratio is firm, to make a stiff divider in this case, it's desired to let a quiescent current pass in the divider that is much larger than the small current supplied by the ADJ pin, this way, variations in the ADJ small current supply wont be able to cause major deviation in the divider's division ratio, which is the desired behavior.

Taking the maximum ADJ current into consideration, that is 120μA, and using the "10 times" rule of thumb someone is able to determine that a voltage divider's quiescent current of 1.2mA will from a relatively stiff divider, so that we might concentrate on letting the quiescent current probably larger than 1.2mA when picking the resistor values. It might also be noted that large transistor values will have the additional advantage, next to reducing quiescent current while meeting the stiffness criterion, of enabling more precise specification of the ratio, and thus will usually enable using 5% tolerance resistors instead of 1% tolerance ones, when resistor values are large enough (in hundreds of kilo ohms). However, since giving a 1.2mA current across a 3.3V source will require a total path resistance of only 2.75kΩ, we will most probably need to use 1% tolerance resistors if we were to have a precise pre – defined ratio.

Picking a regulated voltage of 3.3V, it's apparent that the demanded ratio to the regulated voltage (not to ground) will be V_{ADJ} ÷ 3.3 ≈ 0.38 which means a division ratio to ground of 1 – (this) ≈ 0.62. The standard 5% resistor values 1KΩ and 620Ω achieves this ratio very closely while offering loose tolerances, with a typical ratio of 0.617, a minimum ratio of 0.56, and a maximum ratio of 0.68, giving a worst – case range of regulated voltages of 2.96 to 3.61V, which is nearly identical to the supply range allowed, making the designer feel of almost violating the allowable microcontroller's supply range. Using 1% precision resistors instead, probably with the values 1kΩ ± 1% and 619Ω ± 1%, we can have worst-case range of regulated voltages of 3.199 to 3.342 V which is astonishingly better. Either case, the divider's quiescent current will be nearly 2mA crossing the 1.6mA threshold of the stiffness"10 times" rule-of thumb.

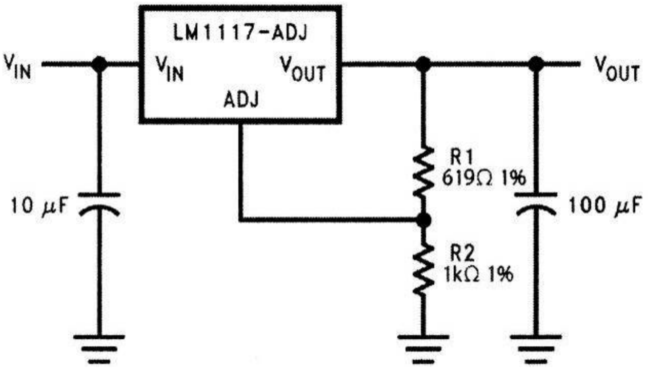

Fig. (1). ResultantSub-circuit: using 1% high-precision resistors.

Another consideration to be made in this design is the maximum junction temperature of the regulator chip, as this chip will be providing current to the whole system including daughterboard(s), which is usually done using the concept of the so-called thermal resistance specified in the datasheets. The thermal resistance Θ is the increase in the junction temperature due to unit dissipation (a single Watt), where the junction is to denote the very small power – dissipating link in silicon whose temperature is an instantaneous function of its instantaneous power – dissipation due to its very small size and trivial heat capacity, this junction is the active element in the device and should be always kept below its maximum allowable temperature, or otherwise the chip will be simply burnt. Thermal resistances are usually specified in a relative manner [4], that is, from junction to case from junction to ambient, and the like, this abstraction is helpful as to ease calculations when someone user a heat – sink mounted on the chip's, package, where in such case, the total thermal resistance is the sum of the thermal resistance from junction to case Θ_{JC}, from the case to the sink Θ_{CS}, and that from the heat – sink to the ambient Θ_{SA}, as it's always required to complete the thermal path from the junction to the ambient. In the case of our design here, we will begin by trying not to use a heat – sink at all, so we can use the specified thermal resistance from the junction to the ambient Θ_{JA} directly, this value is specified in datasheet for each package type as this parameter will obviously vary depending on the package used. For our case here, we use a 3 – lead TO – 220 packages for which Θ_{JA} equals 79°C/Watt, and since we're constrained to maximum current of half an ampere (Maximum USB bus configurable consumption), this implies a maximum dissipation of 3.3V × 500mA = 1.65 Watts, this amount of dissipation will raise the junction temperature by 1.65 × 79°C = 130°C, where the maximum junction temperature is 150°C, which is obviously not acceptable as this will limit the safe operating temperatures to less than the room temperature(25°C). The solution to this problem is using a heat – sink. Nice and neat heat – sinks for the TO – 220 package are very easily obtained and will offer thermal resistances from sink to ambient Θ_{SA} ranging from 4 to 30°C/Watt, and the poorest of which is more than enough to our application here.

Considering the case of a 30°C /Watt sink – to ambient thermal resistance, we can calculate the total thermal resistance as: $\Theta_{JC} + \Theta_{CS} + \Theta_{SA}$ where the junction – to sink thermal resistance for the TO – 220 package of the LM1117 chip is only 3°C /Watt and the thermal resistance from case to sink for the TO – 220 is nearly 0.1°C /Watt if we used a thermally conductive material in between, this gives a total thermal resistance f 3 + 0.1 + 30 = 33.1°C /Watt, this will make the junction's temperature rise by only 55°C instead of 130°C, allowing a safe operation temperatures up to 70°C as to keep the junction's temperature below the recommended level(125°C rather than 150°C of the maximum ratings).

2. Enhanced Microcontroller Support: Apart from the advised sub-circuits mentioned above, there is a good amount of genuine circuitry contained in this work; those are designed to achieve the goal of this main-board as a programmable I/O main-board with development features. They independently work on providing the aid for programmability, basic control needed in development (reset, detach while still powered, etc.), basic status (running in the programming mode, attached, etc.), ad simple development features (programmable LEDs).

2.1. User Reset Single-Shot Generator:

2.1.1. Function: When the user presses the outer momentary button connected to the user-reset pins on the main-board, or manually makes a contact between the two pins of the user-reset momentary. This sub-circuit will work as de-bouncer and a single-shot generator, generation a de-bounced CMOS digital pulse that is no shorter than 1ms in duration, but will stay asserted until the user releases the momentary (i.e. there is no upper bound on the pulse duration, but is guaranteed to last for at least a millisecond).

2.1.2. Operation: This circuit works as a de – bouncer and a single – shot generator (mono – stable multi – vibrator) for the user reset command signal, which is triggered *via* the user reset front – panel V.O. momentary; this is an external normally – open momentary button whose other terminal is connected ground. The single shot generator function is designed as to put a lower bound on the reset pulse width, with no upper bound, as to prevent multiple consecutive resets on long press.

Not that the lower Schmitt NAND is better understood as an active – low OR, while the upper one works more like a NAND, the pin number 5 of the active low Or is tied to a pull – up resistor to V_{DD}, which ensures a low output of the active – low OR when the momentary is not pressed, once the user reset momentary is pressed however, the pin number 5 of the active – low OR is pulled – low with a very small current flowing to ground though through the momentary(275μA), this will cause the output of the active – low OR (C) to become HIGH. When the point C becomes HIGH, this will cause discharging the capacitors of both filter net works A and B (I prefer to consider those charge reservoirs instead of filter network), note that the JFET J1 will ensure an ideal discharge rate since it would turn – off once the discharging begins (J1's gate ground). This way, an ideal discharge rate in both previously charged networks A and B will be issued once the user reset momentary is pressed. Because of the inverter in front of point A (Network A's capacitor voltage), the NAND is expected to be having a HIGH output as long as the both networks are charged (the usual condition), however, once the discharging begin because the user reset momentary has been pressed, this situation changes, Note that network A which has the inverter in front of it will discharge much more rapidly than the other network B, as the capacitor value is one tenth while the resistance value is the same, this will case the inputs of the NAND gate to be both HIGH for a period of time equal to the difference in discharge rates between the two networks, which will result in an active – low single – shot that is nearly equal to the difference in time constants, which means a single shot of around 1ms – 0.1ms ≈ 0.9ms, however, simulation has proved a minimum pulse width that's very close to 1ms (1.0184ms). Not that once the A network discharges, which won't take more than 200μs, self – latching *via* the once considered active – low OR gate will occur and this is how the sub – circuit will have its minimum 1ms pulse even when the user reset command lasts for 200μs, this is also why a shorter press won't be able to trigger a reset, which is the previously mentioned de – bouncing effect.

The result of this discussion is that the de – bouncing effect is proportional to the discharge rate of the A network (the one with the fast discharge rate), and the single – shot effect (minimum pulse duration) is proportional to difference in discharge rate between the two networks, given that there is no upper bound on the pulse duration. Note also that the resulting pulse is inverted, which is why we need inversion to have an active – high version of the single – shot.

2.2. ISP Activation Signal Generator: The is a very simple delay circuit (Fig. **2**) that will delay the falling edge of the active – high version of User Reset Ready by nearly 1ms, causing an ISP activations signal that is issued with the user reset single – shot, but will last for another 1ms(having a minimum duration of 2ms). This ISP activation signal is used to apply the hardware condition that cause the AT89C513A – L to launch in the programming mode. The reason of delay is to allow a satisfactory hold – time so that the hardware conditions get latched correctly on the rising edge of the RESET signal.

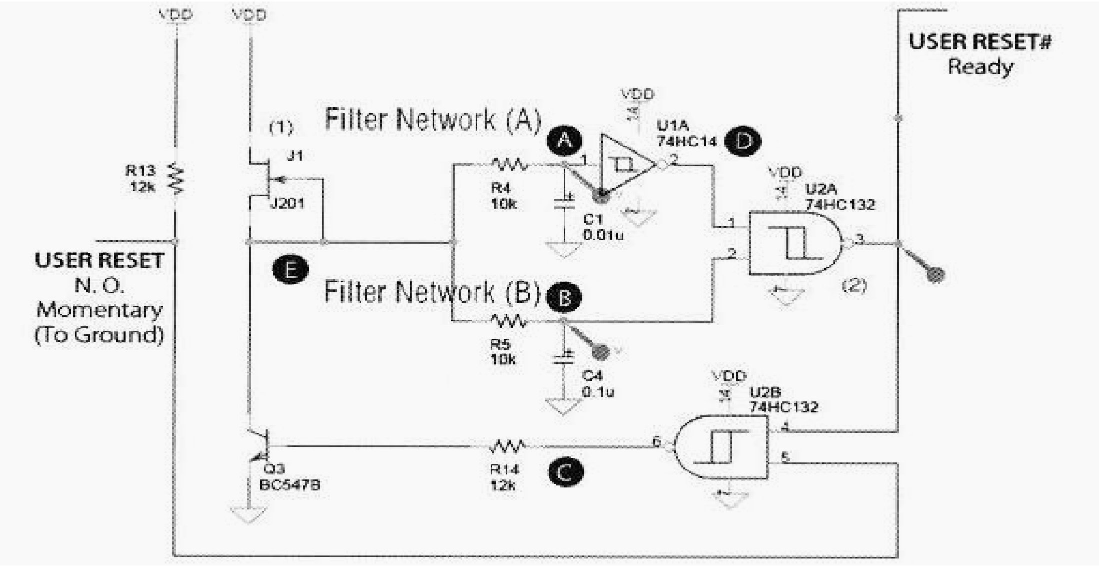

Fig. (2). User reset single-shot generator.

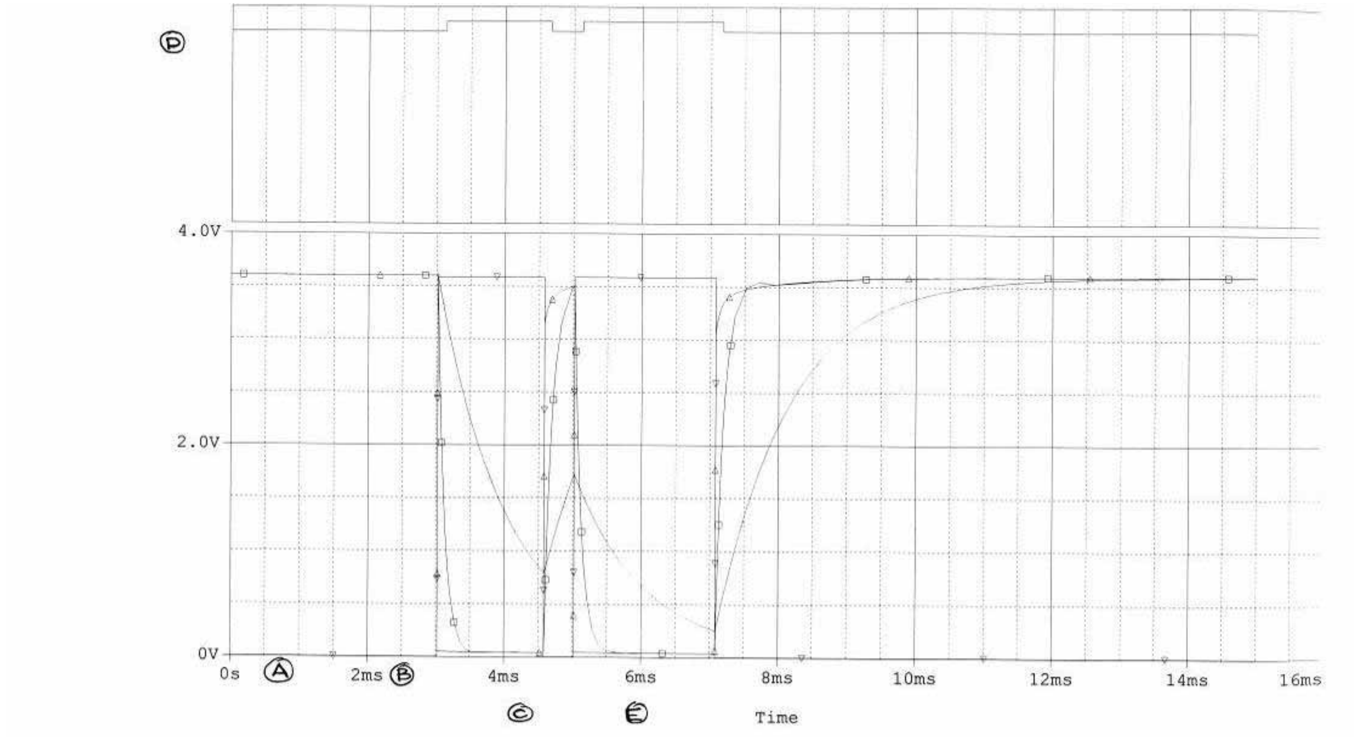

Fig. (3). Simulation results of user reset single-shot generator.

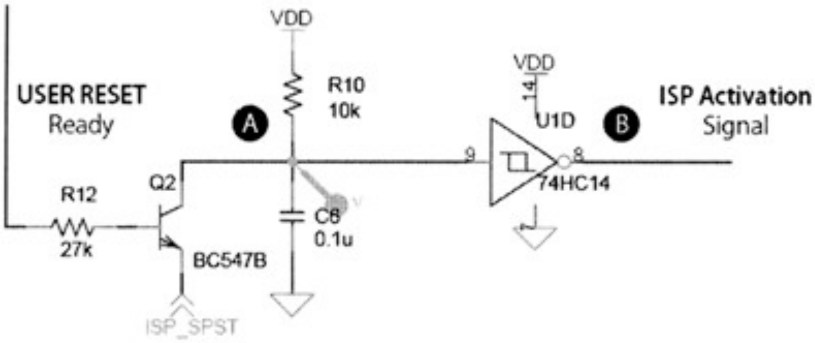

Fig. (4). ISP activation signal generator.

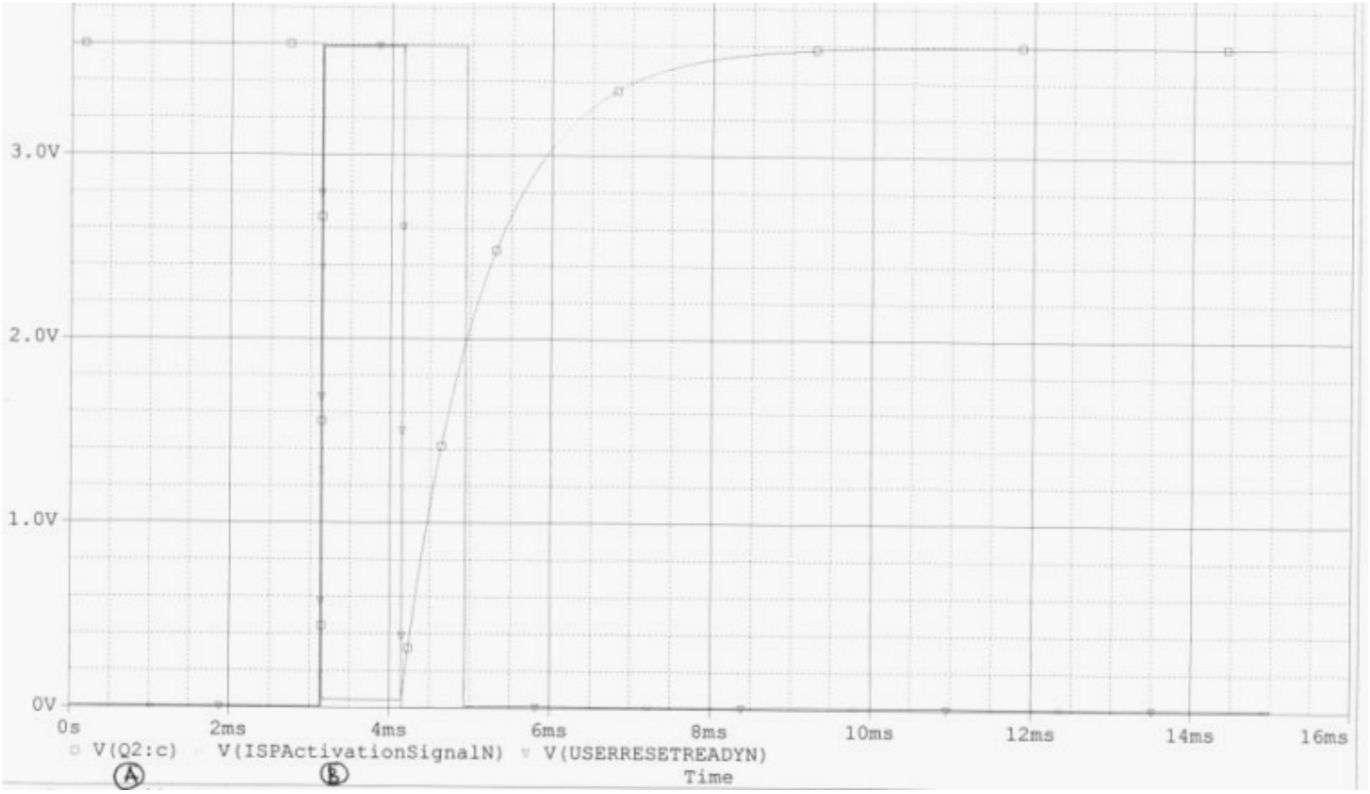

Fig. (5). Simulation results of ISP activation signal generator.

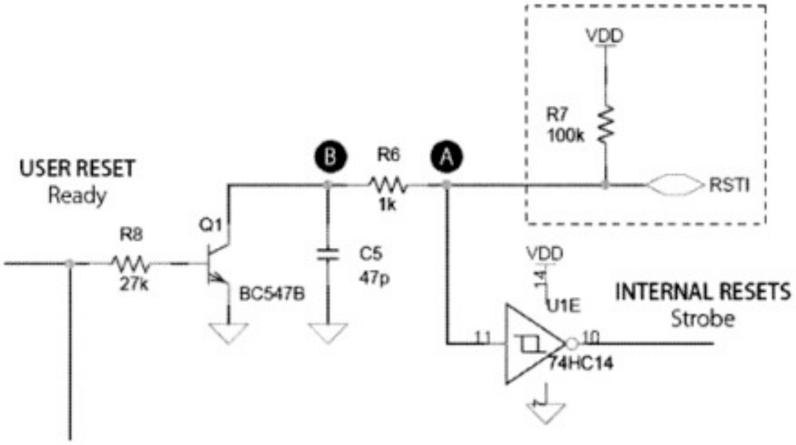

Fig. (6). User reset applier.

***2.3. User Reset Applier*:** This circuit uses a transistor to pull the RST# pin of the AT89C513A – L LOW when a user reset single – shot is issued by the sub – circuit of Fig. (**2**). The region surrounded by the dashed rectangle is a simple model of the RST# pin with its insider 100kΩ typical pull – up, the 1kΩ and the capacitor were recommended in the datasheet of the product [2].

2.4. ISP Hardware Conditions Applier: The main hardware condition to be applied is pulling the PSEN# pin of the microcontroller LOW while reset, it's advised in the datasheet to release this pin after the application of the reset ISP condition as it's normally an output pin, this sub – circuit pulls the pin low using a bipolar transistor, using the user reset single – shot of Fig. (**2**).

This sub – circuit unplugs the D + pull – up of the USB bus, as to cause a short detach while launching the microcontroller chip in the programming mode. This might not be necessary, as it might be implemented automatically in the microcontroller.

This sub – circuit, though not usually necessary, will be needed by someone who uses an external program memory, as the EA# pin when pulled LOW is used as a start – up hardware condition to tell the AT89C513A – L microcontroller to begin execution from an external program memory, rather than running the application stored in its flash program memory.

2.5. Reset Synchronizer [OPTINAL]: This is a very controversial sub – circuit for a number of reasons. First of all, this

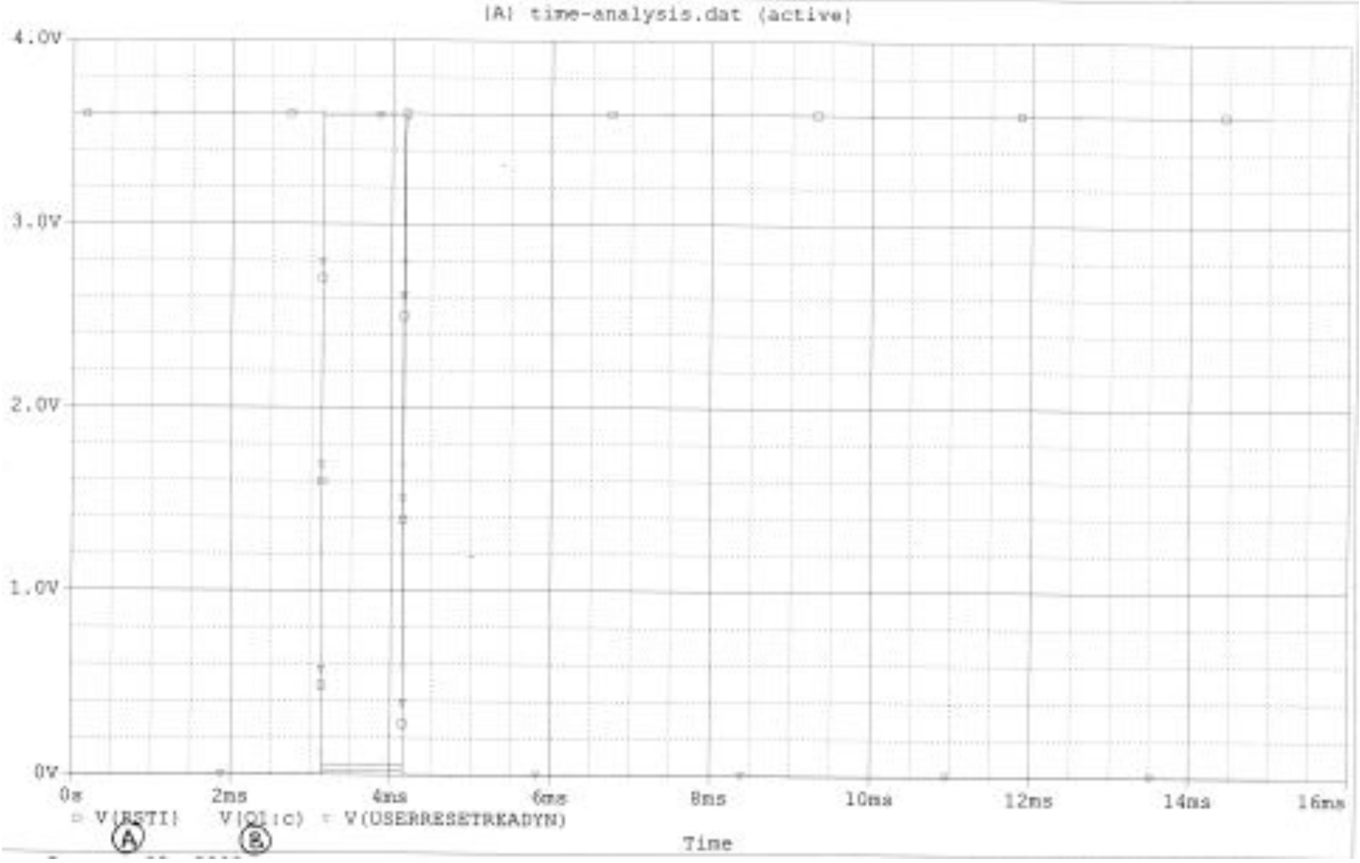

Fig. (7). Simulation results of user reset applier.

circuit is intended to synchronize the externally applied reset rising edge of the RST# pin of the microcontroller with the insider clock of the chip, because of one very annoying bug in a large number of the released chip.

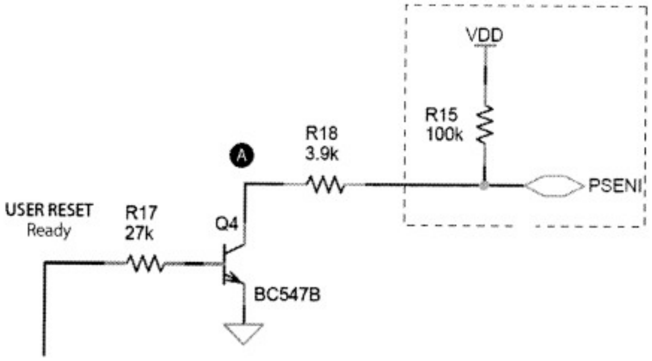

Fig. (8). Hardware conditions applier.

This sub – circuit in brief utilizes a very – fast and power – efficient common – base arrangement that will suddenly discharge a memorizing capacitor on the negative edge of the ALE signal. The ALE signal of the AT89C5131A – L chip is used to multiplex the lower 8 bits of the 16 – bit address with the 8 data bus, this signal happens to be synchronized with the internal clock, which is the how I use it to achieve a synchronized release of the RST# pin of the microcontroller.

After we have achieved a very efficient high – speed discharge of the previously – charged memorizing capacitor, we

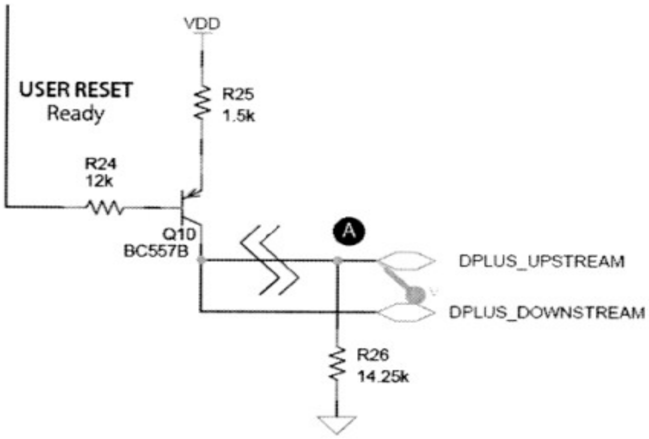

Fig. (9). ISP hardware conditions applier.

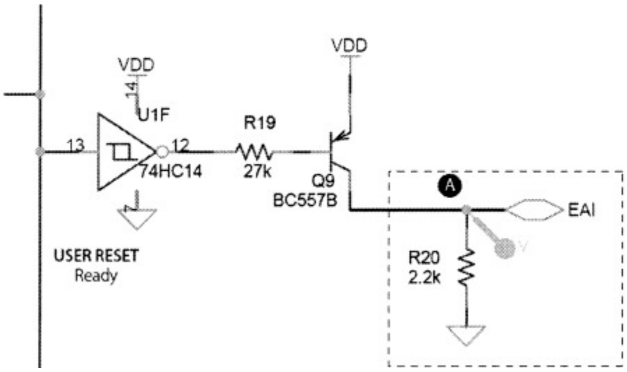

Fig. (10). ISP hardware condition applier.

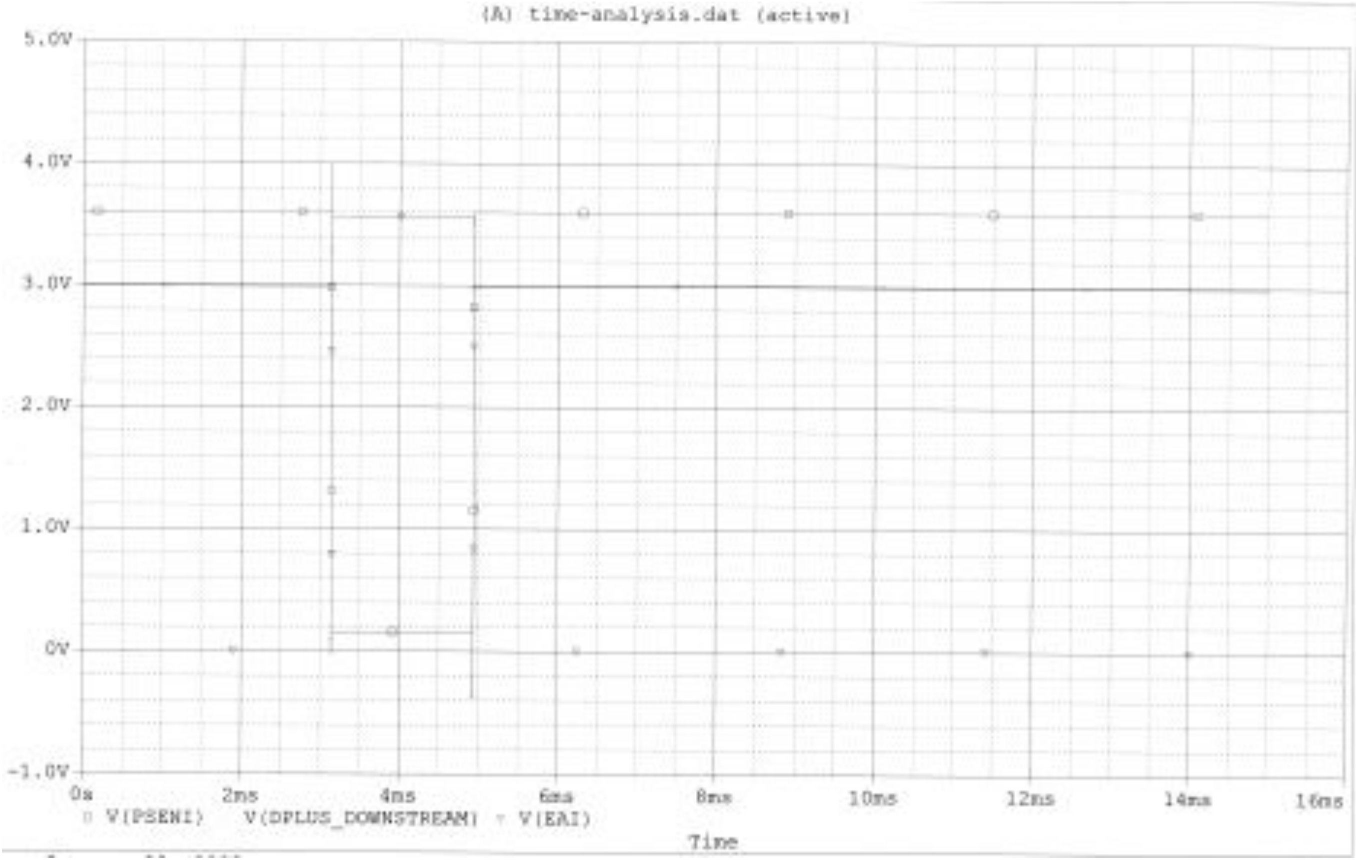

Fig. (11). Simulation results of hardware conditions applier.

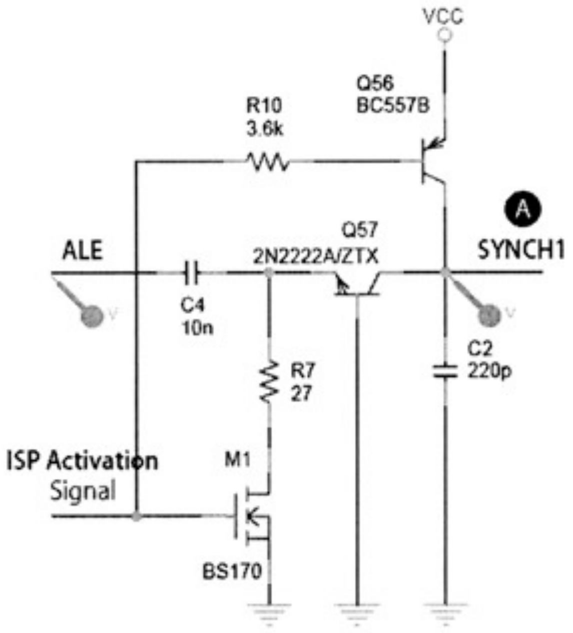

Fig. (12). The User Reset Synchronizer, the first stage negative – edge detector.

use another common – base falling edge detector that will detect this further falling edge can cause a high – speed high – efficiency current sink surge on SYNCH2, similar to the one issued at SYNCH1 previously that cause to immediately discharging the capacitor. The advantage we had from those two stages is a single surge in response to the first negative edge of the ALE signal coming after the user reset has ended, using this sudden current surge at SYNCH2, we need now to very quickly pull the RST# signal up, this active pull – up will cause a rising edge that is very well synchronized with the ALE signal, as the line will take a long time to raise with the passive internal 100k pull – up, the fact that the passive pull – up makes a very slow rise time is well utilized in this circuit to ensure that the RST# will stay low until the active very fast pull – up is applied.

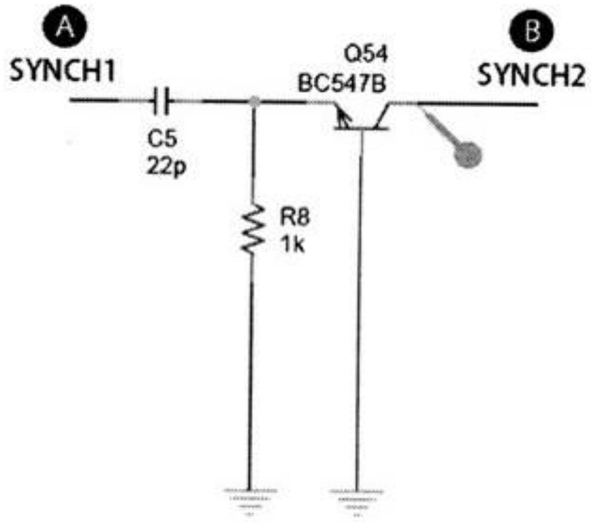

Fig. (13). The User Reset Synchronizer, the second stage negative – edge detector.

This circuit has proved a very satisfactory synchronization in PSPICE simulation, with a total delay of 6ns(from the moment the ALE signal begins to fall until RST# is totally pulled up - HIGH).

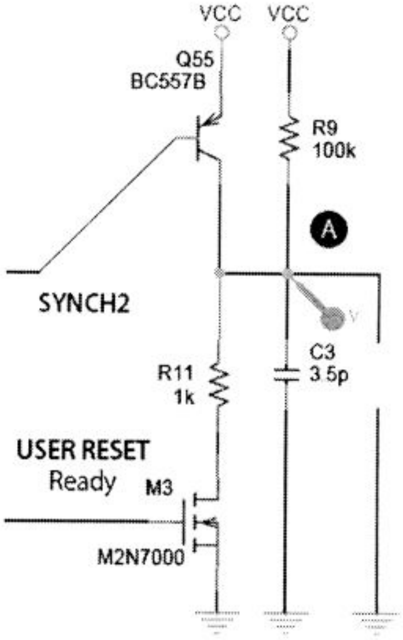

Fig. (14). The user reset synchronizer, the active pull – up.

2.6. Optional Front – Panel LEDs and Switches:_The circuit here remembers the condition of the programming SPST switch at the last reset, and accordingly turns-on a LED to indicate whether we are running in the ISP programming mode or not, this memorizing effect is achieved *via* a thyristor.

2.7. Interface Control Document (ICD)**:** This main-board simply routes all the microcontroller's signals to a modular connector on-board that is to be connected to an external function daughterboard. This choice of the interface signals was made as to allow for the maximum flexibility possible, so that it's possible to use the signals in any manner, as the I/O main-board is also programmable, which makes most flexible arrangement possible.

The modular connector however, can be a lot of things; it can simply be a card – edge (which case daughterboard will more appropriately be called expansion cards), pins – header, or any convenient modular connector.

The chosen connector was the one used for ATA cables inside a PC, this connector uses ribbon cables which are easily obtainable, cheap, and convenient to handle. It also has 40 pins, which is more than the amount needed, as the AT89C5131A – L have 52 pins only 48 of which are meaningful, with less than 38 to be routed, which makes room for passing other special signals of our own, like the previously suggested 3.3V regulated supply.

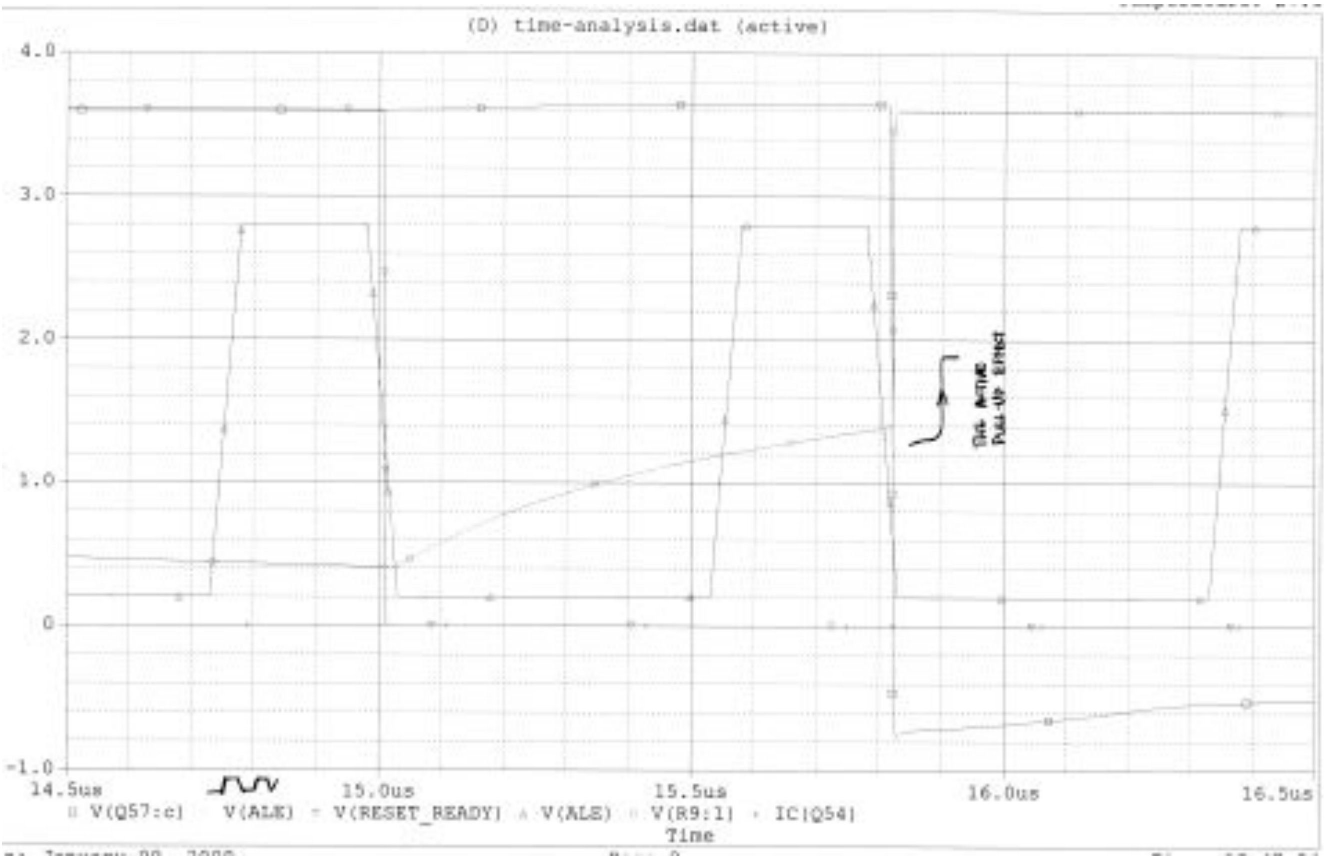

Fig. (15). Simulation results of reset synchronizer.

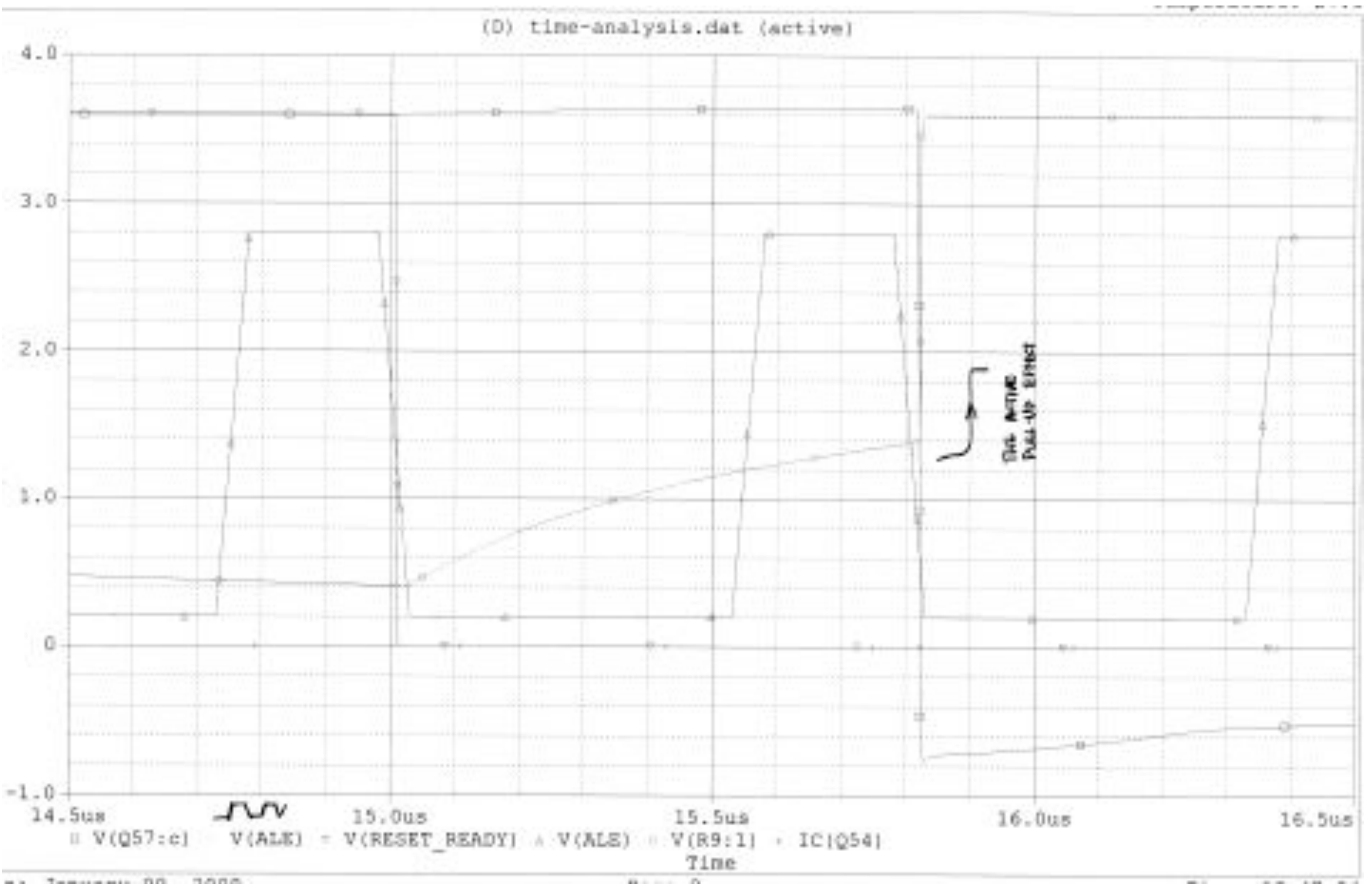

Fig. (15). Simulation results of reset synchronizer.

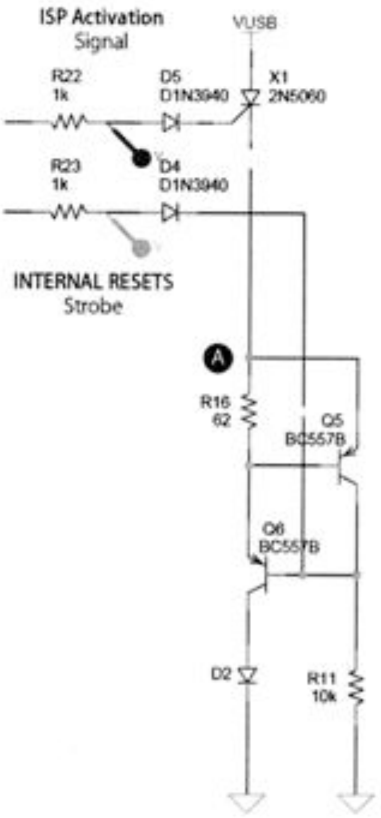

Fig. (16). The ISP mode memorizing LED circuitry.

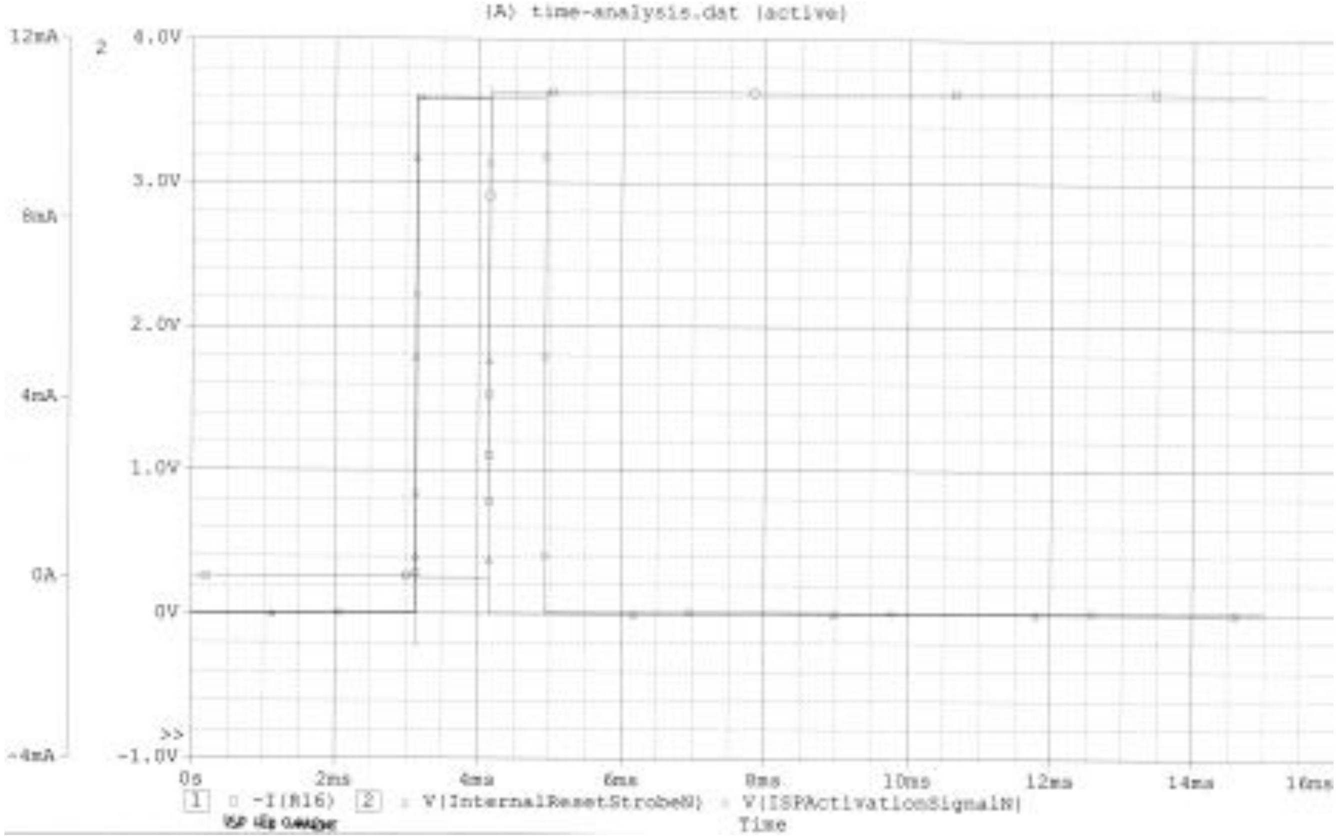

Fig. (17). Simulation results of the ISP mode memorizing LED circuitry.

CONCLUSIONS & FURTHER WORK

Later work, clearly enough, is about developing a function daughterboard that will turn the main-board of this work into a useful end-product. Daughterboard are the boards that get connected to the main-board of this work. Being provided with a regulated supply, fully functional chip with embedded USB controller, and a complete set of signals of the chip providing a good number of services and interfaces (counters, I/O ports, UART, SPI, etc) with the chip (the microcontroller) being specifically programmed for the application, using only the dedicated programming hardware of the main-board, which uses the ISP (In-System-Programming) feature of the chip.

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