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# Modeling and Sizing of Power-Gating Single-Rail MOS Current Mode Logic

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**Abstract:** Almost all power-gating circuits used in MOS current-mode circuits were realized with dual-rail schemes. In this paper, a power-gating scheme for single-rail MOS current mode logic (SRMCML) is presented. The modeling of the sleep transistor in power-gating circuits is constructed and analyzed. The optimization methods for sizing sleep transistors of power-gating circuits are addressed in terms of energy dissipations. The design methods of the power-gating SRMCML circuits are presented. The effectiveness of the proposed power-gating structure is verified by using HSPICE simulations with a SMIC 130nm technology. From the outcomes of simulations, the energy loss of the power-gating SRMCML circuits is smaller than corresponding static CMOS alternatives in high frequencies.

**Keywords:** Low-power electronics, modeling of circuits, power-gating technique, single-rail MCML circuits, sizing of sleep transistor.

## 1. INTRODUCTION

MOS current mode logic (MCML) has the advantage in high frequencies, and thus it is generally used for high-speed applications such as high-speed processors and multiplexers for optical transceivers [1-4]. The power consumption of MCML circuits can be expressed as [5]

$$P = V_{DD} I_B \tag{1}$$

Where, $V_{DD}$ and $I_B$ is source voltage and bias current of the MCML circuit, respectively. From (1), the power consumption of the MCML circuits is constant, since their bias current $I_B$ is a constant operation current in spite of its operating frequencies and activity of input signals. This means that the static power consumption of MCML cells is significantly higher compared with equivalent implementations using conventional static CMOS logic [6].

With the increasing usage of portable and wireless electronic systems, reduction in power consumption of integrated circuits is getting more important than ever [7, 8]. In conventional CMOS circuits, the leakage dissipations can be effectively reduced by introducing power-gating technology [9, 10]. Similarly, idle MCML logic blocks can also be shut down by using power switches to reduce standby power dissipations.

Several power-gating schemes for MCML circuits have been proposed [11, 12]. However, the previously proposed power-gating schemes are almost used for dual-rail MOS current mode logic (DRMCML) circuits. The dual-rail MCML circuits will increase extra area overhead and the complexity of the layout place and route. Moreover, the NMOS series configuration in the dual-rail logic circuits limits the reduction of the minimum supply voltage [13, 14].

The single-rail MCML (SRMCML) circuits were proposed in [13]. The single-rail logic circuits reduce the complexity of the layout place and route, and thus low delay can be expected. In this work, a power-gating scheme for SRMCML is presented. The effectiveness of the proposed power-gating structure is verified by using HSPICE simulations with a SMIC 130nm technology.

This paper is organized as fellow. In section 2, the single-rail MCML circuits are reviewed. In section 3, a power-gating scheme for SRMCML is introduced. The modeling of the sleep transistors in power-gating circuits is also constructed and analyzed in section 3. The results and discussions are incuded in section 4. The conclusions of this paper are given in the last section

## 2. SRMCML CIRCUITS

The conventional dual-rail MCML circuit and its bias circuits are shown in Fig. (**1a**). The DRMCML circuit is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of the NMOS pull-down network (PDN) and its complementary PDN, and the current source transistor Ns. The load transistors are designed to operate at linear region with the help of the control voltage $V_{rfp}$. The PDN and its complementary PDN are used to perform the demanded logic operation. The signal $V_{rfn}$ is used to control the demanded bias current $I_B$, which is mirrored from the current source in the bias circuit.

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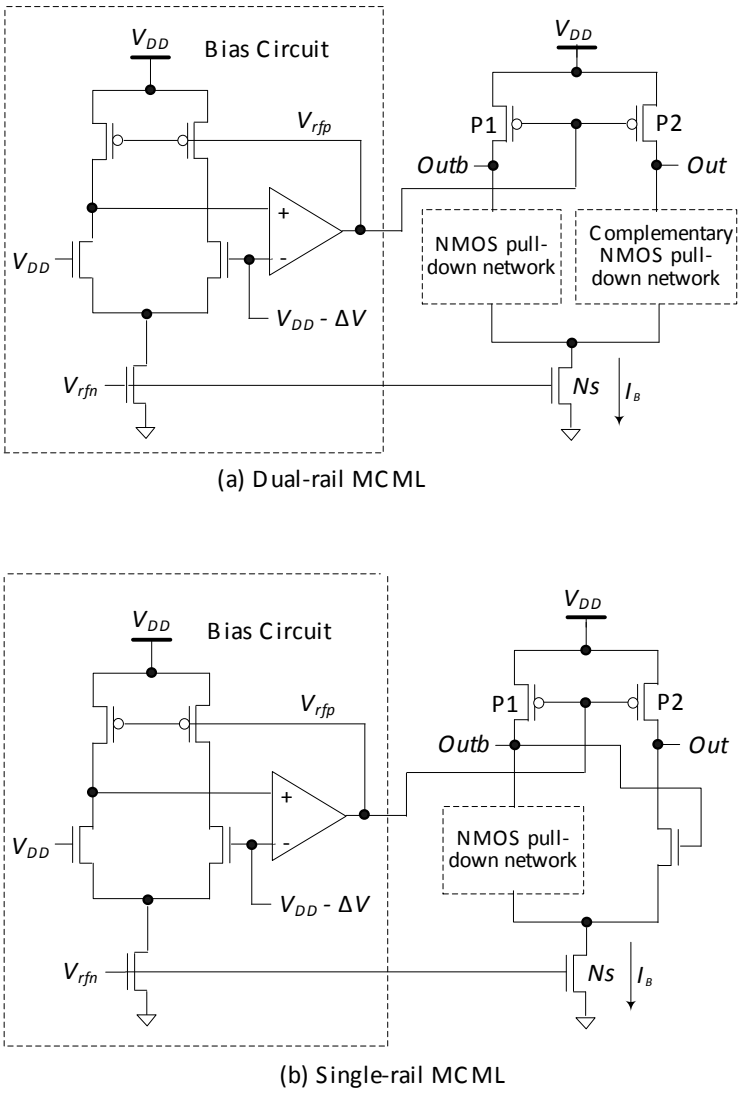


**Fig. (1).** MCML circuits with dual-rail and signal schemes.

The dual-rail MCML circuits increase extra area overhead, because the two complementary PDNs must be used. A single-rail structure of MCML circuits is shown in Fig. (**1b**) [14], which is realized only using a NMOS pull-down network. The complementary NMOS PDN used in the DRMCML circuits is replaced with a NMOS transistor, and its gate is fed back with the output *Outb*.

The basic single-rail MCML gates are shown in Fig. (**2**). The structure of the single-rail MCML circuits is simpler than the dual-rail ones, because only a PDN is demanded. The SRMCML cells can avoid the devices in series configuration, since their logic evaluation block can be realized by only using MOS transistors in parallel. This structure of the single-rail MCML circuits can make their power dissipations to be further reduced, because of low source voltages.

For both DRMCML and SRMCML circuits, the high and low voltages of the outputs are

$$V_{OH} = V_{DD} \text{ and } V_{OL} = V_{DD} - I_B R_D \quad (2)$$

Where, $R_D$ is the linear resistance of the PMOS transistors. The logic swing of the output voltage can be written as

$$\Delta V = V_{OH} - V_{OL} = I_B R_D \quad (3)$$

The proper logic swing $\Delta V$ is obtained by setting the negative-terminal voltage of the operational amplifier in the bias circuits as $V_{DD}$ - $\Delta V$. From (3), for given $\Delta V$ and $I_B$, the linear resistances of the PMOS transistors are determined.

## 3. POWER-GATING SCHEME & MODELING

In this setion, a power-gating scheme for SRMCML circuits is shown in Fig. (**3**). The power-gating SRMCML circuits are composed of the power-gated logic function blocks, power-gating switches, and a bias circuit. The additional high-threshold PMOS transistors (G1-GN) are used to reduce power dissipations in sleep mode, which is inserted between the power supply and power-gated blocks.

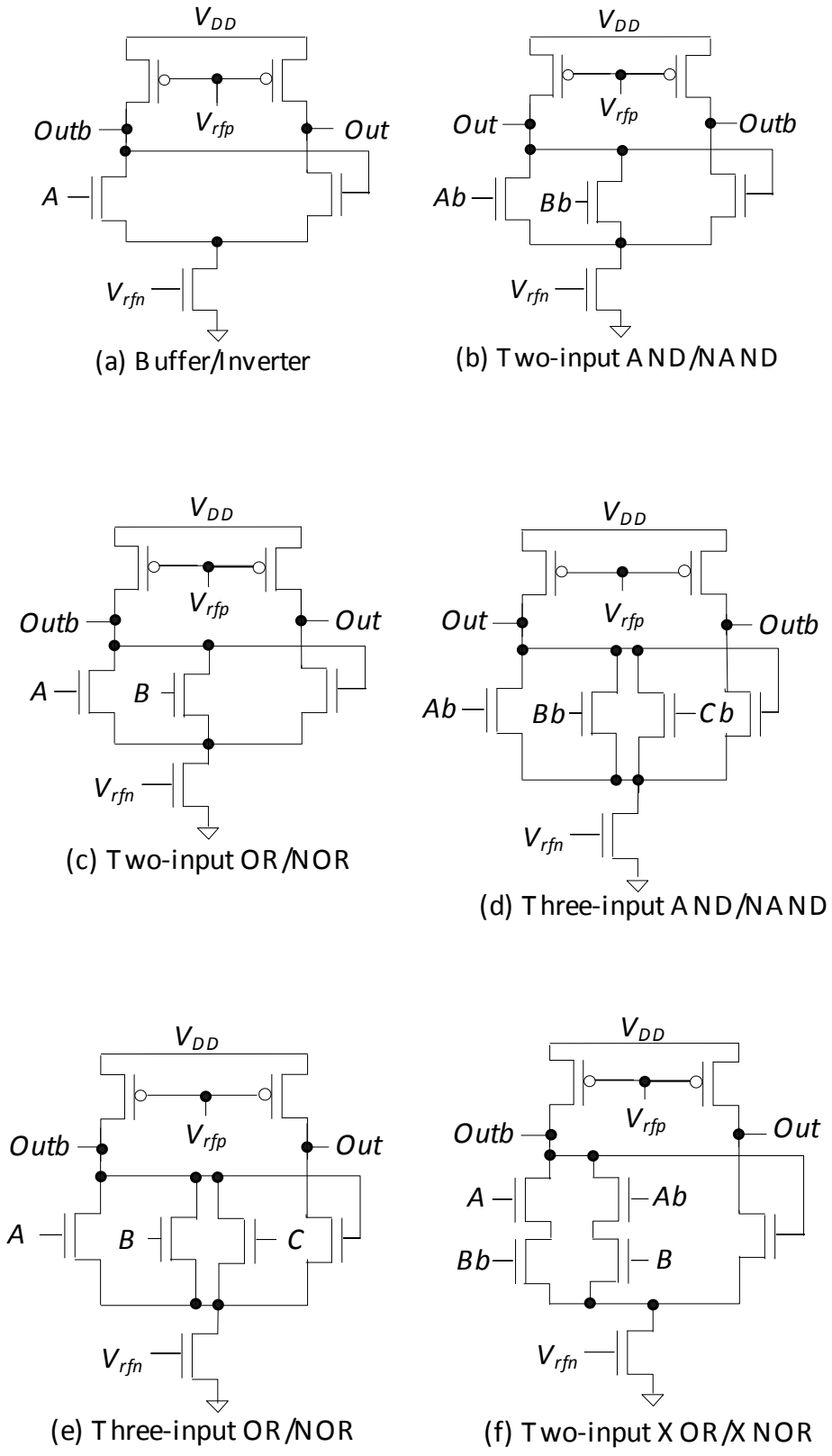


**Fig. (2).** Basic SRMCML gates.

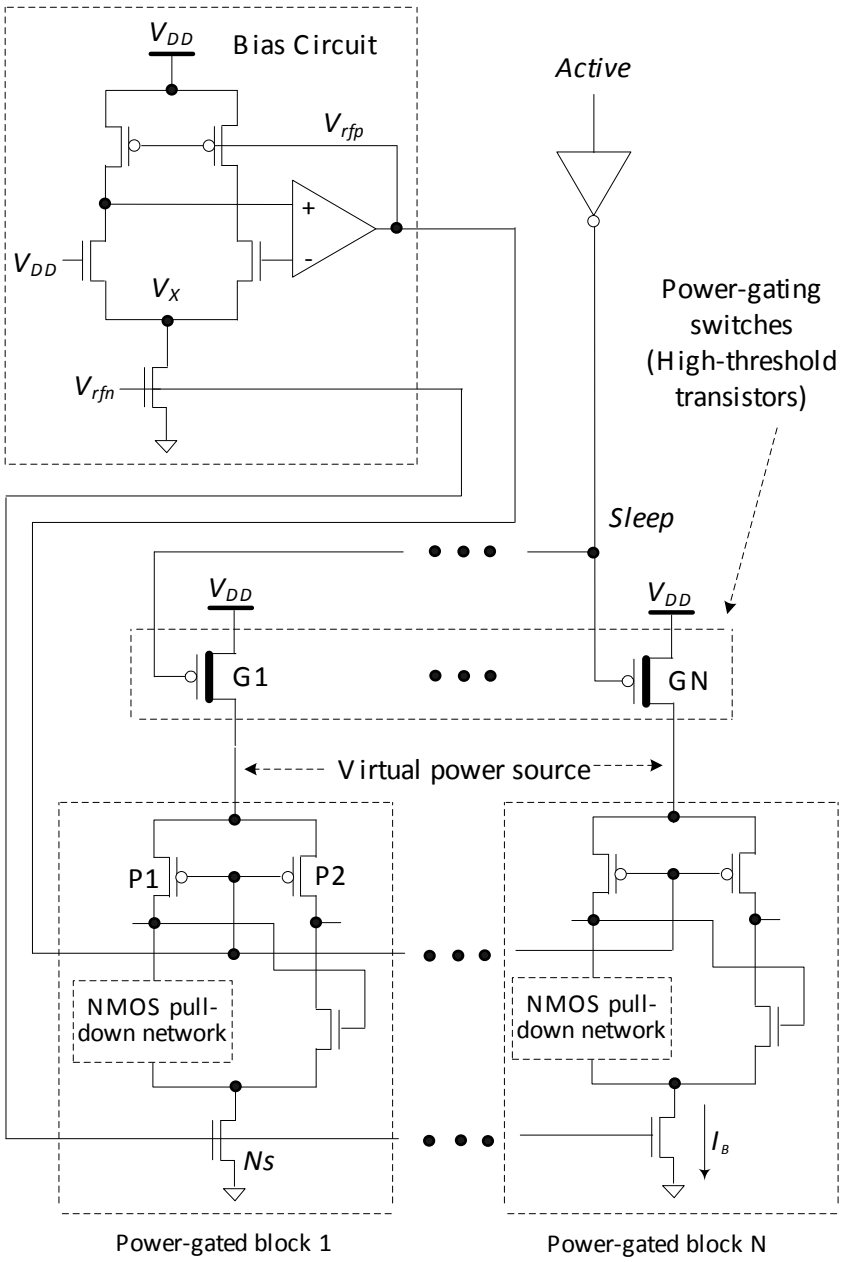


**Fig. (3).** Power-gating scheme for SRMCML circuits.

Power-gating operation schedule is shown in Fig. (**4**). When the input signal Active is set high, high-threshold PMOS transistors G1 - GN are turned on, and thus SRMCML circuits works in active mode. If the signal Active is low, G1 - GN are turned off, the power supply of the SCMCML logic blocks are shut down, and thus SCMCML circuits operates in sleep mode. In power-gating circuits, not all function blocks are shut down at the same time. At this time, the power-gated blocks should be severely power-gated by introducing additional Active signals.

Additional power-gating switches shall cause energy overhead, which should be analyzed and optimized. In a power-gating period, the total energy loss $E_{total}$ is the sum of the energy loss $E_{active}$ in active time $T_{active}$, the energy dissipation $E_{sleep}$ in sleep time $T_{sleep}$, the energy consumption $E_{on}$ for turning on the power-gating switches, and the energy loss $E_{OFF}$ for shutting down the power-gating switches. In the following sub-sections, these energy dissipations are analyzed and investigated in detail.

As shown in Fig. (**3**), in the active mode, the current that flows through the power source $V_{DD}$ is a constant current $I_B$. The equivalent circuit for calculating the energy dissipation of the power-gating circuits is shown in Fig. (**5**).

The energy loss per period in active mode can be written as

$$E_{active} = V_{DD} I_B T \tag{4}$$

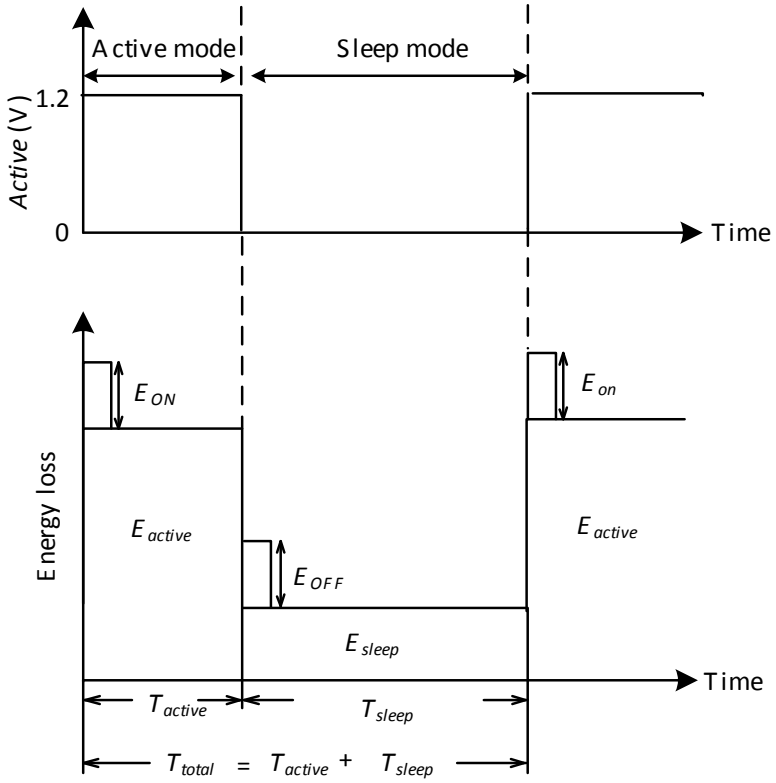


**Fig. (4).** Operation schedule and energy loss of power-gating SRMCML circuits.

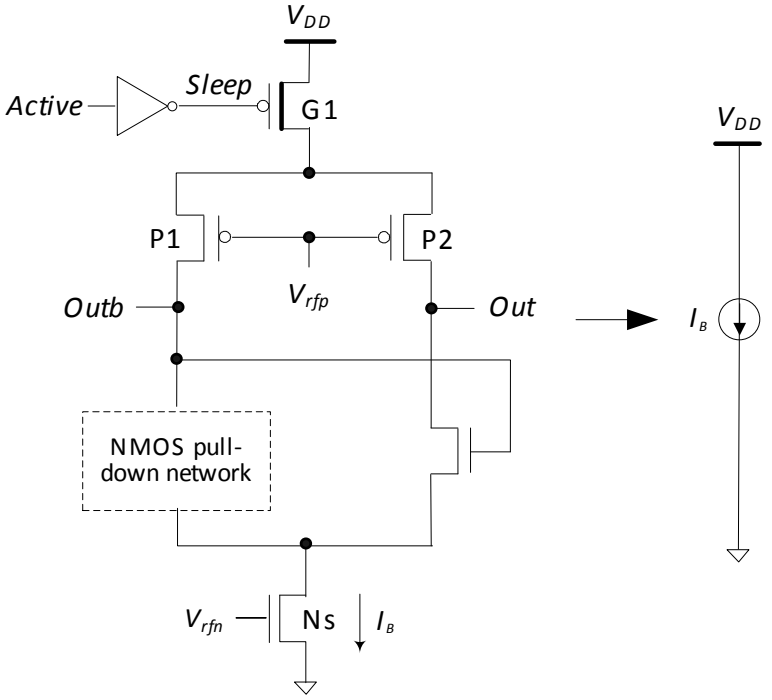


**Fig. (5).** Equivalent circuit for calculating the energy dissipation of the power-gating circuits in active mode.

Where, $T$ is the clock period. The simulations for energy losses of the power-gating circuits have been performed, as shown in Fig. (**6**). In these simulations, the channel length of the power-gating transistor G1 was taken with 10λ (λ = 65 nm), and the channel width of the power-gating switch G1 ranges from Wnor to 8×$W_{nor}$, where $W_{nor}$ is 16λ. The bias current $I_B$ was set as 20 μA. The working frequency $f$ is 100 MHz. Fig. (**6**) shows that energy loss $E_{active}$ almost keeps constant as the size of the power-gating transistor is varying.

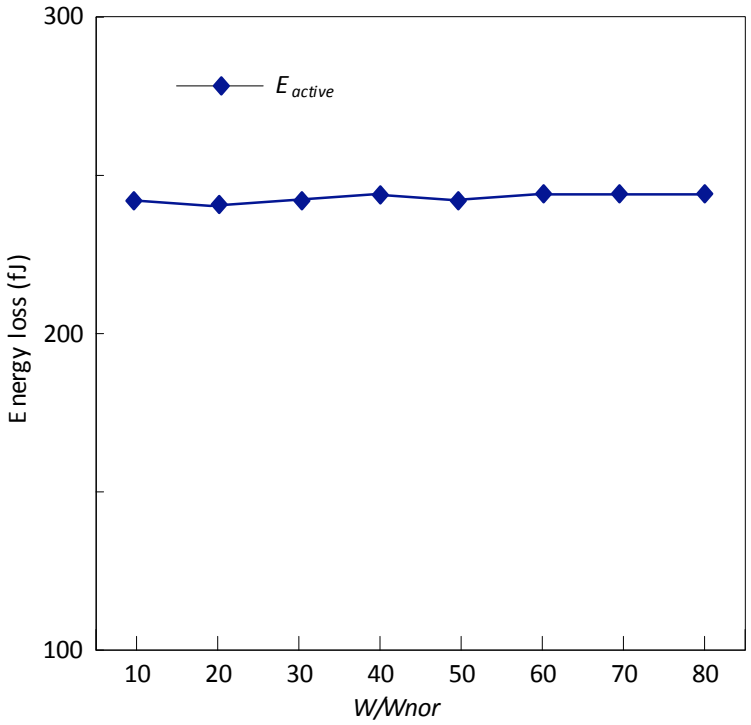


**Fig. (6).** Energy loss *versus* channel width of the power-gating switch G1 in active mode. $W_{nor}$ is 1.04 μm.

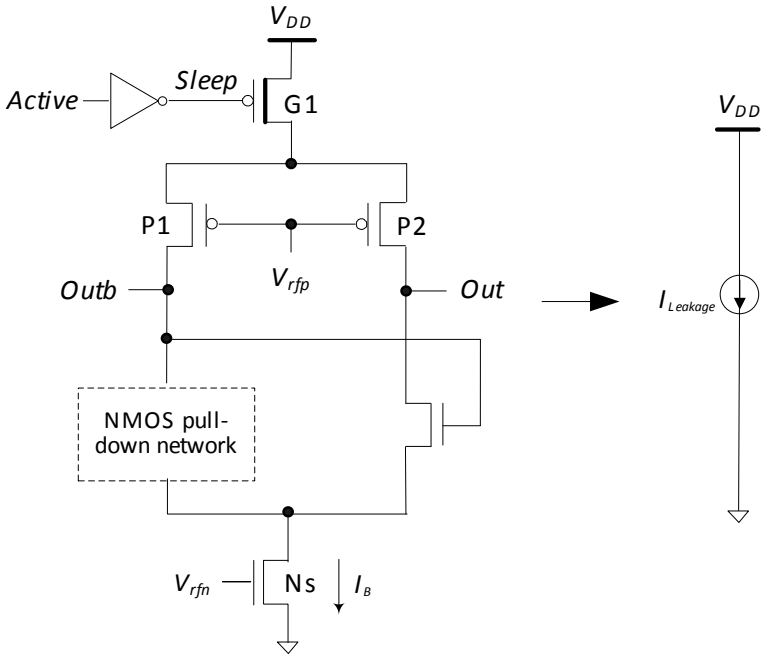


**Fig. (7).** Equivalent circuit for calculating the energy dissipation of the power-gating circuits in sleep mode.

When the power-gating switch operates in sleep mode, the power-gating switch is turned off, and the MCML block is shut down. The current that flows through the power source $V_{DD}$ is only leakage of the power-gating transistor G1. The equivalent circuit for calculating the energy dissipation of the power-gating circuits in sleep mode is shown in Fig. (**7**). The energy loss per period in sleep mode can be written as

$$E_{sleep} = I_{leakage} V_{DD} T \quad (5)$$

Where, $I_{leekage}$ is the leakage current of the power-gating PMOS transistor. At current level of CMOS technology, the sub-threshold leakage current exponentially decreases as the threshold voltage is increased. In fact, increasing the threshold voltage by 100 mV decreases the leakage current by a factor of about 10. Moreover, in short channel MOS

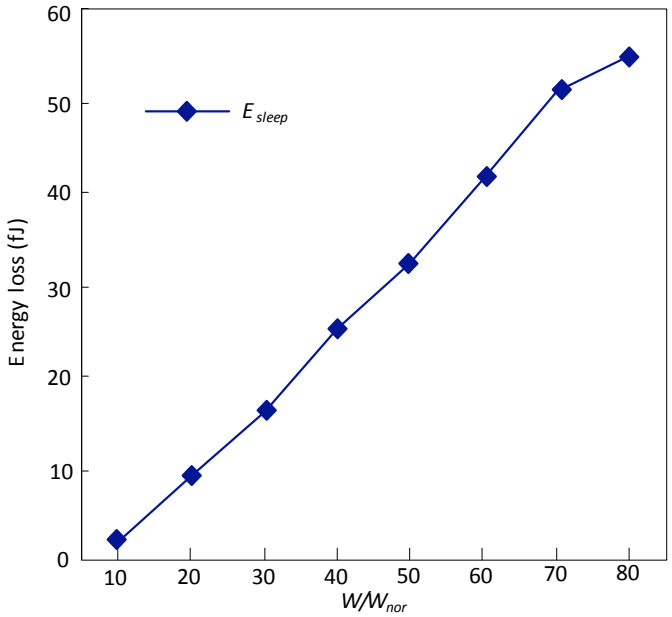


**Fig. (8).** Energy loss *versus* channel width of the power-gating switch G1 in sleep mode. $W_{nor}$ is 1.04 μm

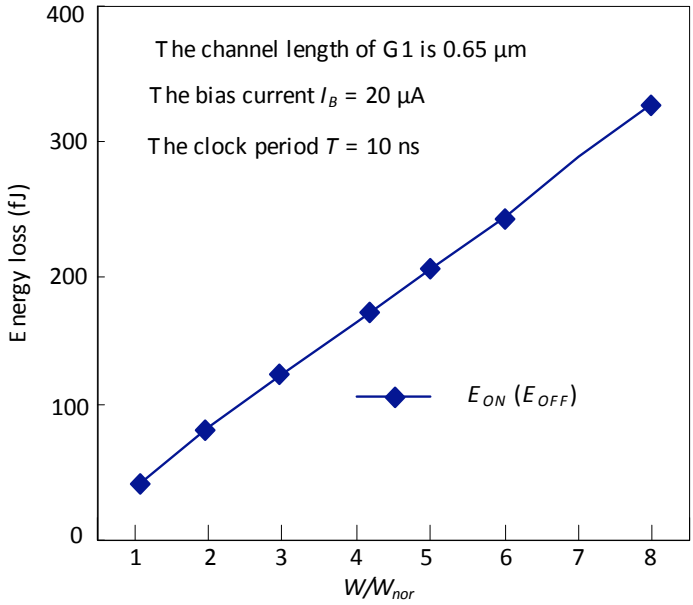


**Fig. (9).** Energy loss for turning on and off the power-gating switch G1 *versus* channel width of the power-gating transistor. $W_{nor}$ is 1.04 μm.

transistors, the threshold voltage of the transistor dependens on its channel length. Therefore, in order to reduce the leakage current of the power-gating transistor, a large channel length should be used with an accepted area penalty. In our design, the channel length of the power-gating transistor G1 was taken as 0.65 μm (10λ).

The simulations for energy losses of the single-rail power-gating circuits in sleep mode have been carried out, as shown in Fig. (**8**). The leakage energy loss $E_{sleep}$ is proportional to the channel width of the power-gating transistor G1. $E_{active}$ is about 100 times of $E_{sleep}$ when the channel width of G1 is $W_{nor}$, and the bias current is 20 μA.

The energy dissipation of the power-gating circuit in sleep mode increases as the channel width of the power-gating transistor increases. $E_{sleep}$ is almost independent of the bias current. These conclusions prove the correctness of the theories.

In order to turn on and off the power-gating switches between sleep mode and active mode, additional energy will be dissipated. The node Sleep is charged from $V_{DD}$ to 0V for turning on the power-gating switch, while the node $X$ is charged from 0V to $V_{DD}$ for turning off the switch. Therefore, energy losses for turning on and off the switch can be written as

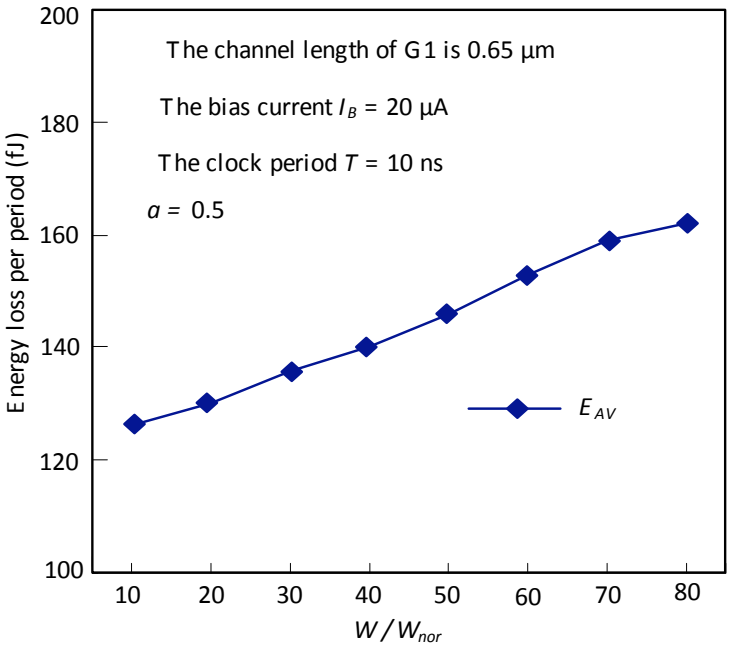


**Fig. (10).** Average energy loss per period of the power-gating circuits *versus* channel width of the power-gating transistor. $W_{nor}$ is 1.04 μm.

$$E_{ON} = E_{OFF} = (1/2)C_{G1}V_{DD}^2 \quad (6)$$

Where, $C_{G1}$ is the capacitance of the node *Sleep*. Fig. (**9**) shows the simulation results of the switching energy loss $E_{ON}$ ($E_{OFF}$). Just as expected, the energy loss $E_{ON}$ ($E_{OFF}$) is proportional to the channel width of the power-gating transistor G1.

Combining (4), (5), and (6), total energy loss of the power-gating circuits in a power-gating period can be written as

$$E_{total} = E_{active}(\frac{T_{active}}{T}) + E_{sleep}(\frac{T_{sleep}}{T}) + E_{ON} + E_{OFF} \quad (7)$$

Average energy loss per period of power-gating circuits can be expressed as

$$E_{AV} = \frac{E_{total}}{(T_{active} + T_{sleep})/T} = (E_{active})\alpha + E_{sleep}(1-\alpha) + \frac{E_{ON} + E_{OFF}}{(T_{active} + T_{sleep})/T} \quad (8)$$

Where, α is power-gating active ratio that is defined as $\alpha = T_{active}/(T_{active} + T_{sleep})$. When $T_{sleep}$ is long enough, the energy loss ($E_{ON}$ + $E_{OFF}$) can be ignored, and thus $E_{AV}$ can be rewritten as

$$E_{AV} \approx (E_{active})\alpha + E_{sleep}(1-\alpha) \quad (9)$$

For given source voltage $V_{DD}$, operating frequency $f$, and bias current $I_B$, the energy dissipation $E_{active}$ keeps constant according to (4). The energy dissipations $E_{sleep}$ decreases by reducing its channel width according to (5), and (6). Therefore, in order to minimize the energy overhead, the channel width of the power-gating transistor G1 should be as small as possible. Moreover, as mentioned above, in order to reduce the leakage current of the power-gating transistor, a large channel length may be used with an accepted area penalty. In this work, the channel length of the power-gating PMOS transistors G1 was taken as 10λ. In this case, small channel width would result in the voltage degradation of the virtual power source. Therefore, a minimum channel width of the power-gating transistor is limited. In this work, the minimum channel width of the power-gating transistor G1 was taken with $W_{nor}$ (16λ).

Fig. (**10**) shows the simulation results of the energy loss $E_{AV}$ per period of the power-gating MCML circuits. In these simulations, the bias current IB is also set as 20 μA. The channel length of the power-gating switch G1 was taken as 10λ. The working frequency is 100MHz. The power-gating activity was taken as 0.5. As shown in Fig. (**10**), the average energy dissipation per period is proportional to the channel width of the power-gating switch G1.

## 4. RESULTS & DISCUSSIONS

Taken as an example, the design, optimization, and energy dissipations of a 1-bit SRMCML full adder are addressed in detail. The logic function of the 1-bit full adder can be expressed as

$$S = A \cdot Bb \cdot C_i b + Ab \cdot B \cdot C_i b + Ab \cdot Bb \cdot C_i + A \cdot B \cdot C_i$$

$$C_O = A \cdot B + B \cdot C_i + A \cdot C_i \quad (10)$$

Where, A, B, Ci are input signals, CO is carry signal, and S is sum signal, respectively. According to (10), the full adder based on the power-gating SRMCML scheme is shown in Fig. (**11**).

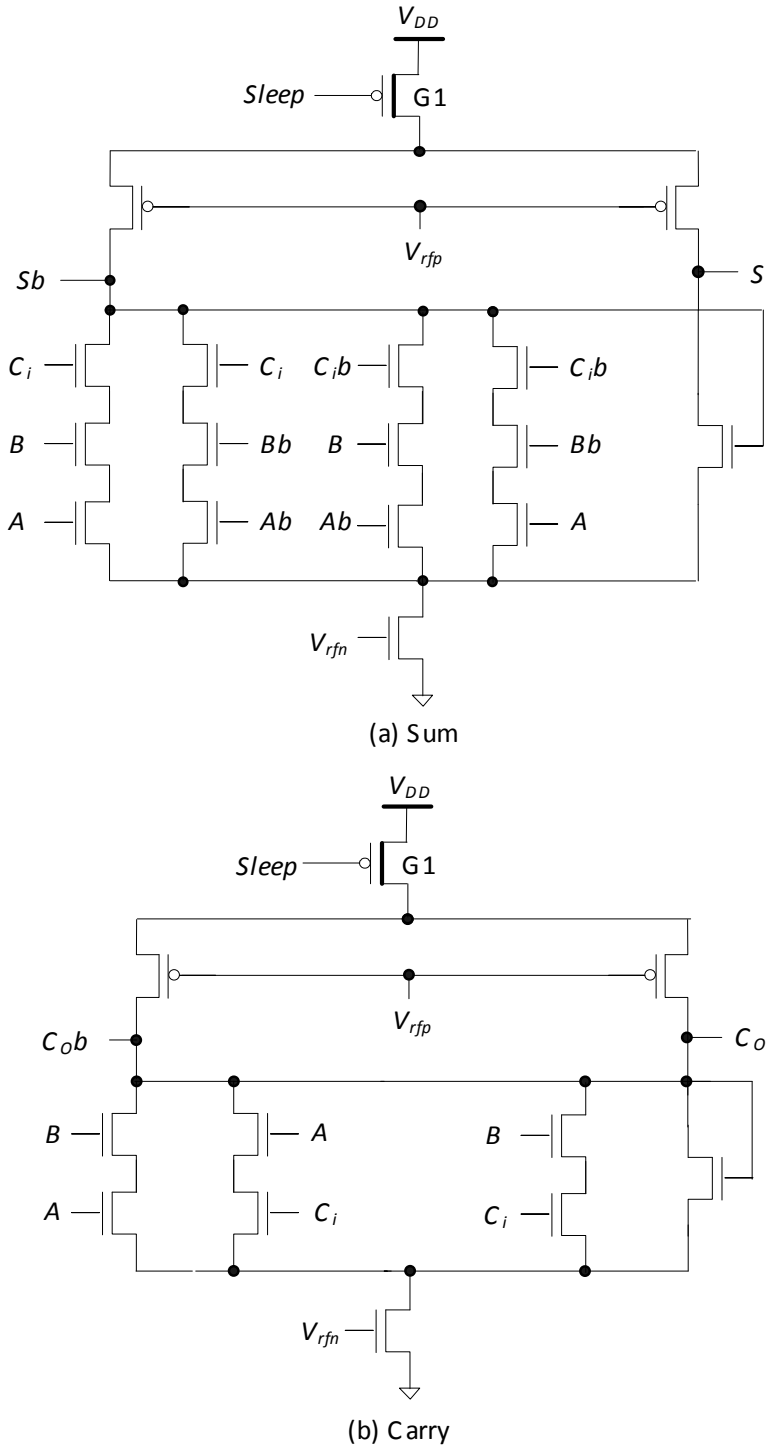


**Fig. (11).** Power-gating 1-bit full adder based on SRMCML.

The power-gating SRMCML full adder has been simulated by using HSPICE at the 130nm CMOS process. Fig. (**12**) shows its simulated waveforms. As is shown in Fig. (**12**), the adder has correct logic functions.

For comparison, the 1-bit full adder based on the conventional CMOS using the PMOS power-gating has been also simulated at the same CMOS technology. The power dissipations of the power-gating SRMCML and conventional CMOS full adders are compared in Fig. (**13**). In these simulations, the operation frequency ranges from 200 MHz to 3 GHz. The power-gating active ratio $\alpha$ of both SRMCML and conventional CMOS full adders is 50%. The device size of the power-gating PMOS transistor G1 was taken with $W/L$ = 16λ / 10λ (λ=65nm). The bias current $I_B$ of the SRMCML adder is set as 20 μA.

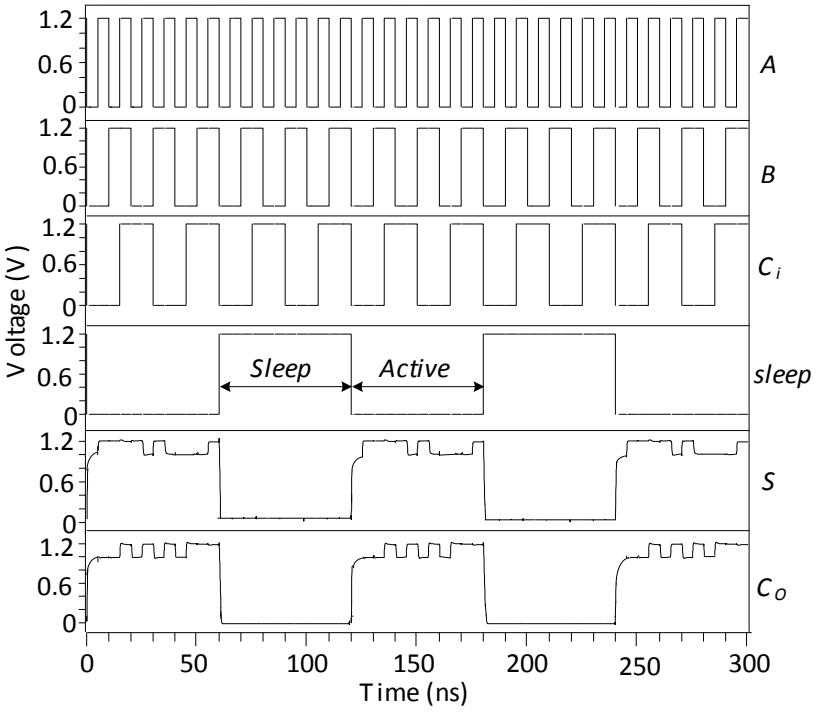


**Fig. (12).** Simulation waveforms of the power-gating 1-bit full adder based on SRMCML.

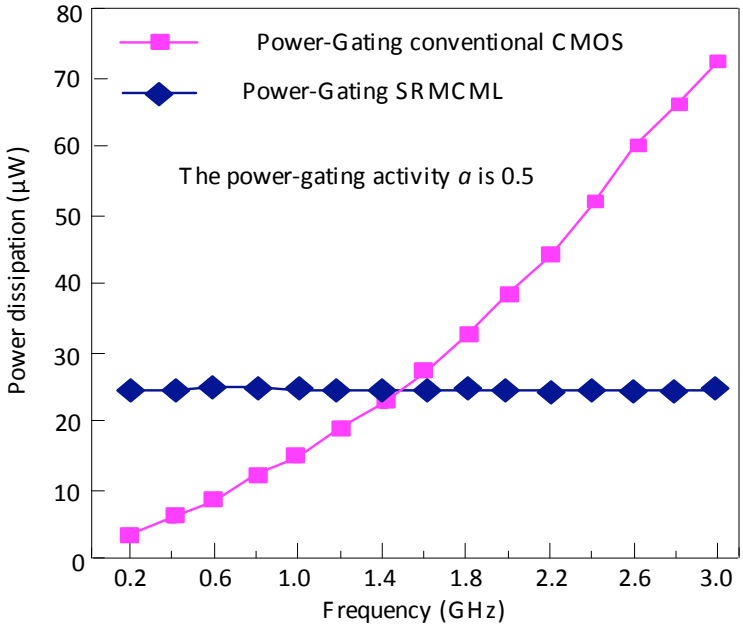


**Fig. (13).** Power consumption comparison between the power-gating SRMCML and conventional CMOS full adders.

Just as expected, the power consumption of the MCML adder is almost independent of operating frequency, while the power consumption of the conventional CMOS adder increases linearly with the operating frequency. From Fig. (**13**), the power consumption of the SRMCML adder is lower than the conventional CMOS one and in terms of operating frequencies larger than about 1.5 GHz. At 3 GHz operating frequency, the power dissipation of the power-gating SRMCML adder is only about 35% of the power dissipation of the conventional CMOS power-gating one.

The power dissipations of the power-gating circuits depend strongly on the power-gating active ratio according to (9). The power dissipations of the power-gating SRMCML adder with various activities are shown in Fig. (**14**).

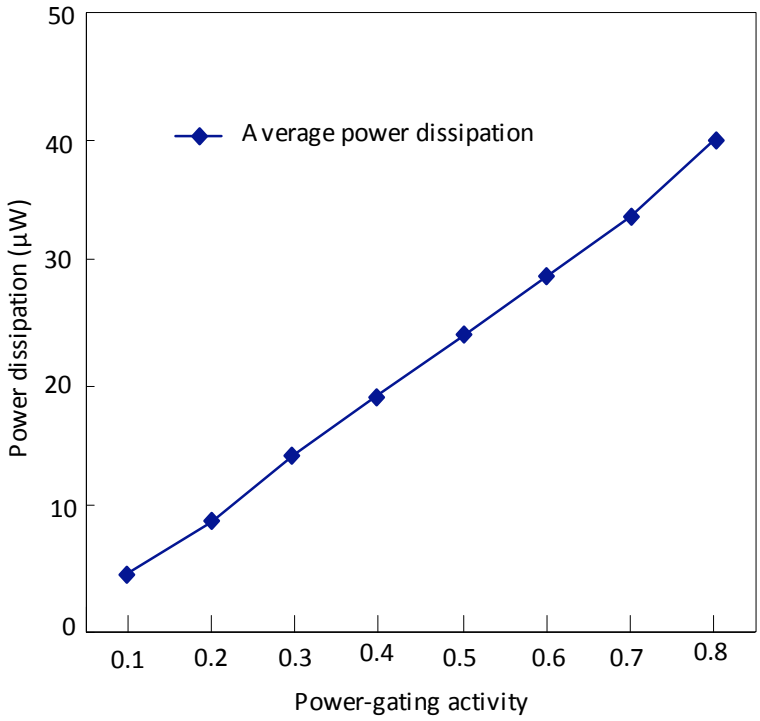


**Fig. (14).** Power dissipations of the power-gating SRMCML full adder with various power-gating active ratios.

The power-gating active ratio ranges from 0.1 to 0.8. In these simulations, the device size of G1 was taken with $W/L = 16\lambda/10\lambda$ ($\lambda = 65$ nm), and the bias current was set as 20 μA.

As mentioned above, when the device size of the power-gating transistor is taken with $W/L = 16\lambda/10\lambda$, and the bias current is 20 μA, $E_{sleep}$ is only about 1% of $E_{active}$. Therefore, for the power-gating activity larger than 0.1, the average energy dissipation of the power-gating SRMCML circuits can be rewritten as $E_{AV} \approx (E_{active})\alpha + E_{sleep}(1-\alpha) \approx E_{active}a$. Therefore, the average energy dissipation of the power-gating SRMCML circuits is proportional to power-gating activity, and accordingly its power dissipation depends linearly on the activity. Just as the theoretical analysis, Fig. (**14**) shows that the power dissipation of the power-gating SRMCML adder decreases linearly with the reduced activity

## CONCLUSION

The structure of the power-gating scheme for single-rail MOS current mode logic (SRMCML) has been presented. The modeling of the sleep transistors in power-gating circuits is constructed and analyzed in detail. The optimization methods of power-gating circuits have to be also addressed in tern of energy dissipations. The design methods of the power-gating MCML circuits using the single-rail scheme are also presented. HSPICE simulations show that the power dissipations of the power-gating SRMCML circuits are smaller than corresponding static CMOS alternatives in high-speed applications.

## CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

## ACKNOWLEDGEMENTS

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