Theoretical Model of Signal Transmission Based on Digital Radio Receiver

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Abstract: Radio receiver, as an extensively feasible modern technology, has been widely applied in all fields of military and civil. It is mainly to demodulate all kinds of required signals with strong interference and noise. Based on intermediate frequency (IF) software radio receiver test platform, the data transmission approach combining direct memory access (DMA) and multichannel buffered serial port (McBSP) was studied and the parallel operation of data transmission and data processing was realized. The method proposed for signal transmission and processing shows strong universality and can be used in other relevant fields.

Keywords: Radio receiver, Digital signal, Signal transmission, Data processing.

1. INTRODUCTION

Receiver, as a critical element in radio communication, once developed from the primary regenerating receiver and direct receiver to the later super heterodyne receiver and zero- intermediate frequency (IF) receiver, and now, software digital radio receiver system has been the most popular one. Recently, with the rapid technological development, particularly the development of chip integration and digital technology, higher requirements are put forward for receiver mechanism. As radio digital receiver for real-time signal transmission and processing has to accomplish large data transmission and signal processing operation in limited time simultaneously, reasonable and effective algorithm is very important, so does the selection of practical data transmission method. However, the time for data transmission commonly exceeds that for data processing in practical, which is a difficulty in the development of real-time signal processing system. Based on IF software radio receiver test platform, the research introduced bidirectional data transmission technology that combines direct memory access (DMA) and multichannel buffered serial port (McBSP) [1-5].

2. IF SOFTWARE RADIO RECEIVER

The core concept of software radio receiver is to maintain A/D and D/A converters at a closer distance to the antenna and realize more software radio functions using the software. Based on software radio concept and the processing ability of current A/D converter and digital signal processer (DSP), IF software digital radio receiver obtains digital signals by sampling and quantizing signals received by the antenna at IF; then it realizes corresponding signal filtering and demodulation by using different software of the universal DSP. The receiver is characterized by universality and flexibility [6].

IF software digital radio receiver test platform is illustrated in Fig. (**1**). In the figure, AD6640 module is a single channel high speed A/D chip of 12-bit 65MSPS (million samples per second), which can directly sample and quantize IF modulating signal; AD6620 module is a programmable digital down converter of 16-bit 67MSPS, which down-converses and filters the signal and reduces data rate by receiving the 12-bit high speed data signal in parallel way exported by AD6640 module. The PC of the test platform operates AD6620MicroPort by using the parallel port and performs online programming for the internal register of AD6620 module. AD6620 and AD6640 modules operate simultaneously by using same external clocks. TMS320C6701, as a high speed floating-point DSP with a maximum processing capacity of 2400 MOPS, is designed for transmitting and demodulating digital signals.

3. SIGNAL SAMPLE THEORY

The core idea of software digital radio receiver is to directly perform digital processing for the radio frequency analog signals received by antenna as early as possible, and convert the signals to data stream that suitable for DSP or computer [7]. Finally it realizes all kinds of functions using software (algorithm) and presents better scalability. Therefore, the first problem of software digital radio receiver is how to digital process the analog signals within the working band (for example, in a range of 0.1MHz~2GHz).

3.1. Nyquist Sampling (Lowpass Sampling)

The basic idea of Nyquist sampling theorem is described as follows [8]: to begin with, a frequency band-limited signal is set, whose frequency band is limited within $(0, f_H)$; then equal interval sampling is conducted for the frequency band-limited signal at a rate no less than to obtain the sampling signal (where is called sampling interval) which disperses at equal time; then the original frequency band-limited signal is

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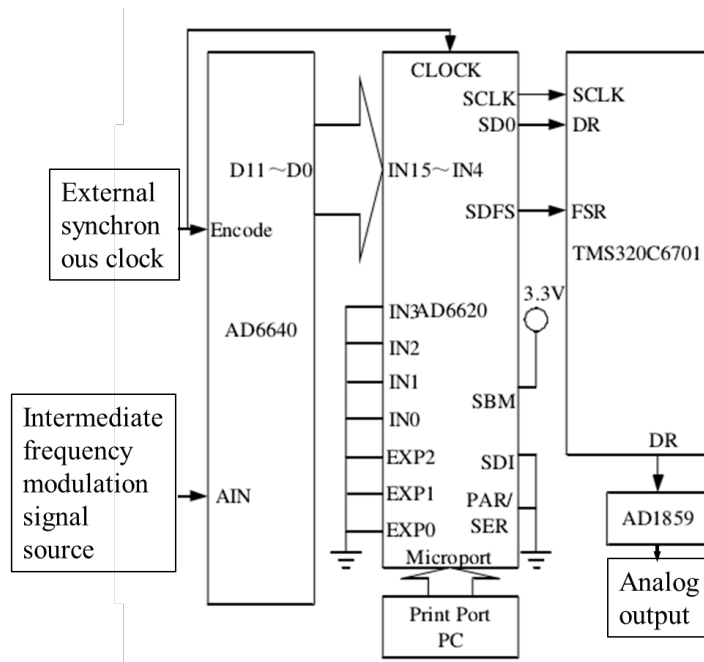E-mail: houyanxy@163.com

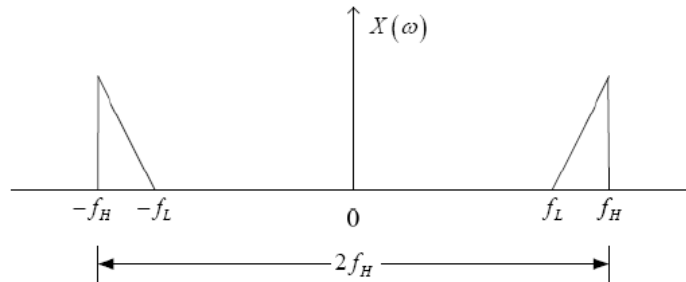**Fig. (1).** IF software digital radio receiver test platform.

Fig. (2). Frequency spectrum of band-pass signal.

completely determined by the obtained sampling value $x(n)$. The sampling theorem is represented by

$$x(t) = \sum_{-\infty}^{+\infty} x(n) Sa(\pi f_s t - n\pi) \qquad (1)$$

Formula (1) indicates that as long as $f_s \geq 2f_H$, the frequency band-limited signal can be accurately determined using its sampling value $x(n)$. It implies that when samples the frequency band-limited signal at a rate not less than two times of the highest frequency of the signal, the obtained discrete sampling accurately determined the original signal. That is, discrete sampling value is able to replace the consecutive analog signals, which lays the theoretical basis for the digital processing of analog signals [9, 10].

3.2. Band-Pass Signal Sampling Theory

Assuming there is a frequency band-limited signal $x(t)$, whose frequency bandwidth is limited in (f_L, f_H). Band-Pass

signal sampling theorem [11] is described as, if its sampling rate meets the following formula, the original frequency band-limited signal can be accurately determined by the sampling value that obtained by the equal interval sampling of f_s.

$$f_s = \frac{2(f_L + f_H)}{2n+1} \qquad (2)$$

Where n is the maximum positive integer that satisfies $f_s \geq 2(f_H - f_L)$. When expressed by the center frequency of the Band-Pass signal and the bandwidth B, Formula (2) is represented as

$$f_s = \frac{4f_o}{2n+1} \qquad (3)$$

Where $f_o \geq (f_H + f_L)/2$, n is the maximum positive integer meets (B is bandwidth). Obviously, when and $B = f_H$, Formula (3) is Nyquist Band-Pass sampling theorem.

Suppose that the frequency spectrum of the Band-Pass signal is demonstrated in Fig. (**2**), the higher and lower cut-
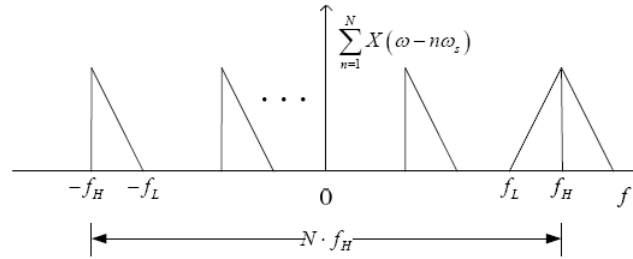
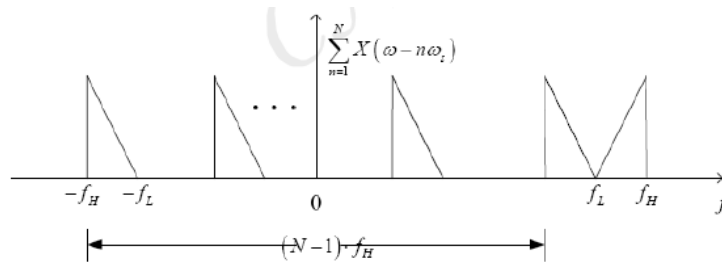**Fig. (3).** Frequency spectrum after sampling.

Fig. (4). Frequency spectrum after sampling.

off frequencies of the signal are and f_L, respectively, then the bandwidth is $B = f_H - f_L$. Without loss of generality, the Band-Pass signal is rewritten as $f_H = N \cdot B + M \cdot B$, where N is positive integer and M is decimal that less than 1 (0≤M≤1).

Fig. (**3**) illustrates that to avoid aliasing for spectral components and minimize the sampling rate f_s, the following requirement has to be satisfied:

$$N \cdot f_s \geq 2 f_H \tag{4}$$

Where and [ ] indicates it is an integer.

As the sampling frequency increases continuously, to avoid aliasing of the spectrum (as shown in Fig. **4**), the sampling rate has to meet:

$$(N-1) \cdot f_s + 2B \leq 2 f_H \tag{5}$$

Formulae (4) and (5) indicate that to avoid aliasing for the frequency spectrum, the sampling rate has to meet

$$\frac{2 f_H}{N} \leq f_s \leq \frac{2(f_H - B)}{N-1} \tag{6}$$

To guarantee Band-Pass under sampling principle, the maximum sampling rate has to meet

$$f_s + 2B \leq 2 f_H \tag{7}$$

As the sampling rate reduces continuously, to avert aliasing for the frequency spectrum, the sampling rate has to satisfy

$$f_s \geq f_H \tag{8}$$

According to Formulae (7) and (8), to avoid aliasing, the sampling rate requires to satisfying

$$f_s \geq f_H \tag{9}$$

Therefore, it is inferred that

$$\frac{2 f_H}{n} \leq f_s \leq \frac{2(f_H - B)}{n-1} \tag{10}$$

Where 2<n<N.

By integrating Formulae (6), (9) and (10), Band-Pass under sampling principle can be uniformly expressed as

$$\frac{2 f_H}{n} \leq f_s \leq \frac{2(f_H - B)}{n-1}, 2<n<N \tag{11}$$

Band-Pass sampling merely allows signals on one of the band, instead of signals on different bands simultaneously; otherwise, there will be aliasing of the signals. Therefore, in the sampling of a Band-Pass signal at certain center frequency, the signal can be modulated to corresponding center frequency using anti-aliasing filter first, then the interested Band-Pass signals are filtered, and finally the signals are sampled using the Band-Pass sampling theorem.

4. DATA TRANSMISSION COMBINING DMA AND MCBSP

4.1. McBSP Set

TMS320C6701 provides three high-speed McBSPs, which provide transmit register with double buffers and receive register with three buffers. Therefore, McBSP shows the function of full-duplex synchronous or asynchronous communication and allows continuous transmission of data
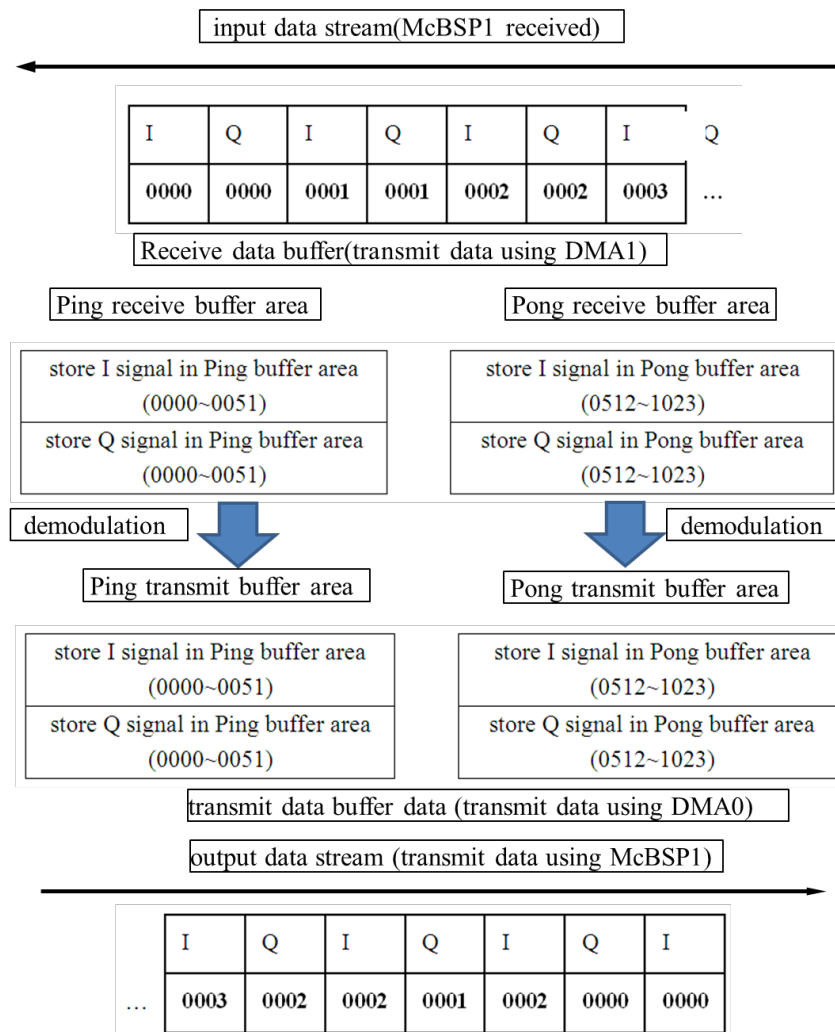
input data stream(McBSP1 received)

I	Q	I	Q	I	Q	I	Q
0000	0000	0001	0001	0002	0002	0003	...

Receive data buffer(transmit data using DMA1)

Ping receive buffer area   Pong receive buffer area

store I signal in Ping buffer area (0000~0051)	store I signal in Pong buffer area (0512~1023)
store Q signal in Ping buffer area (0000~0051)	store Q signal in Pong buffer area (0512~1023)

demodulation   demodulation

Ping transmit buffer area   Pong transmit buffer area

store I signal in Ping buffer area (0000~0051)	store I signal in Pong buffer area (0512~1023)
store Q signal in Ping buffer area (0000~0051)	store Q signal in Pong buffer area (0512~1023)

transmit data buffer data (transmit data using DMA0)

output data stream (transmit data using McBSP1)

I	Q	I	Q	I	Q	I
...	0003	0002	0002	0001	0002	0000	0000

Fig. (5). Ping-pong buffer based data transmission.

stream. There are independent programmable frame synchronization signals for data transmission and data receive. Additionally, McBSP can directly connect to decoder and analog interface chip of industrial standard or other serial A/D converter, A/D converter, and SPI devices. It supports external clock input or internal programmable clock. Each serial port can support data transmission and receive of 128 channels at most. The serial character length is optional from 8, 12, 16, 20, 24, and 32-bit. Furthermore, McBSP supports the compressing and expansion of A-law data.

McBSP connects with peripheral equipments by 7 pins including DX, DR, CLKX, CLKR, FSX, FSR, and CLKS. DX and DR pins show the function of data transmission and receiving in the communication with peripheral equipments; CLKX, FSR, FSX, and CLKR control the synchronization of clock and frame; CLKS provides system clock. When transmit data, CPU and DMA write data for transmitting in DXR (data transmission register); under the effect of FSX and CLKX, DX pin outputs data. When receive data, under the effect of FSR and CLKR, DR pin reads data from DRR (data receive register). The receiving and transmission of frame synchronous impulse can be realized by internal sampling

rate generator and be motivated by external impulse source as well; while McBSP accomplishes data detection on the rising edge and the fall edge of corresponding clock, respectively.

Serial port control register (SPCR) and pin control register (PCR) are designed to fulfill operations of serial port. Receiving control register (RCR) and transmission control register (XCR) set received parameters and transmitted parameters, including frame length, respectively. In the software digital radio receiver test platform, DSP and AD6620 are connected according to the serial communication method (PAR/SER=0), and AD6620 module operates in main mode (SBM=1) and sends clock synchronization signal SCLK and frame synchronization signal SDFS to feedback shift register (FSR); simultaneously, McBSP1 receives the service data objects (SDO) sent by AD6620 to data recorder (DR).

4.2. DMA Set

TMS320C6701 provides four independent self-loading DMA channels for DMA data transmission and an assistant DMA channel for communicating with the main machine.

DMA controller is able to move data in the mapping storage space without using CPU resource. Each DMA channel can set operation mode according to the main control register, source address register, global index register, secondary control register, destination control register, and global address register. In the test platform, by combining DMA and McBSP1, bidirectional transmission of data is realized.

DMA1 restores the data in McBSP1DRR to internal high-speed storage area to be demodulated by DSP and its synchronization event is the receiving event of McBSP1 (REVT1); at the same time, DMAO transmits data that demodulated by DSP in the internal high-speed storage area to the DXR of McBSP1 to be output by D/A, and its synchronization event is the transmission event of McBSP1 (XEVT1). By combining DMA with the data transmission of McBSP, DSP is gotten rid of frequent task of serial port data processing, and it can be totally applied in the demodulation thereby.

4.3. Double-indexing Sort

Double-indexing, as a unique technology of DMA, it extracts and sorts same types of data from those interleaving access ones. Double-indexing is used because some peripheral equipments output two signals. For example, voice signal is coherent with modulation signal. But the processer merely processes one of the two signals once. While DMA is able to automatically sort the received data using double-indexing characteristic, instead of the intervention AD6620 module in the test platform divides the modulation signal to orthogonal signal Q and in-phase signal I; the data of serial output are in the format of a logic frame, which contains two elements, namely, a group of orthogonal signal Q and a group of in-phase signal I with 16 bits of each group. As CPU processes a signal each time, it extracts in-phase signal I from the continuously interleaving signals and places it in the upper half part of the data buffer, and extracts orthogonal signal Q and places it in the lower half part of the data butter, to be demodulated by DSP, respectively. The concrete process is as follows: CEI register of DMA stores the position increment of buffer pointer in the receiving of in-phase signal I, that is, the buffer pointer jumps forward half buffering area; CFI register of DMA stores the position increment of buffer pointer in the receiving of orthogonal signal Q, that is, the buffer pointer jumps back half buffer area to the end of the buffer area in the receiving of in-phase signal last time. The operation is repeated.

4.4. Ping-Pong Buffer

Ping-Pong buffer is a data transmission technology applying two data buffer areas simultaneously. Ping-Pong buffer is used because data are likely to be overwritten in data transmission and processing with single buffer. While the continuous operation of Ping-Pong buffer keeps an acti-

vated buffer area for data transmission and a static buffer area for data processing using DSP. The data transmission process using Ping-Pong buffer method is demonstrated in Fig. (**5**).

CONCLUSION

Based on Nyquist and Band-Pass signal sampling theory, data transmission technology combining DMA and McBSP was investigated, the setup and management for McBSP and DMA using DSP/BIOS real-time operation system were analyzed, and the embedded signal demodulation method was proposed. The research realized the parallel operation of data transmission and data processing.

CONFLICT OF INTEREST

The author confirms that this article content has no conflicts of interest.

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