The organization of this paper is as follows. In Sect. 2, a three-stage step-up resonant switched capacitor (RSC) converter is briefly reviewed. It is considered as a typical example of zero-current switching. To reveal the SOMs in the studied RSC, an automated approach based on Boolean matrix is described in Section 3. A detailed dynamical study is then carried out in Section 4. The condition of the occurrence of SOM is mathematically deduced, and it is confirmed both in experiments. Finally, conclusions are drawn in Section 5.

2. A ZERO-CURRENT-SWITCHING CONVERTER

Fig. (1) depicts a three-stage step-up resonant switched capacitor (RSC) converter utilizing zero-current switching [14]. The switching devices Q1 and Q2 are power MOSFET shunted by its body diode. A resonant inductor Lr is connected in series with the switching capacitors C1 and C2, forming the resonant unit to create zero-current switching. The duty cycle of operation is designed as 50% while the switches Q1 and Q2 are turned ON and OFF alternatively with a period of Tr.

Fig. (2) depicts the normal output waveforms of the RSC converter where four operational modes, denoted as Modes I–IV, based on the corresponding topological states, can be identified.

A. Mode I [t=t0~t1]

Switch Q2 and diodes D1 and D2 are turned on at t0 with zero-current. In this mode, C1 and C2 are charged up by the input source Vx and the charges stored at Cb1, respectively, while the power for the load Rl is supplied by Cb2. Eventually, the voltages across C1 and C2, denoted as Vc1 and Vc2, reach their maximum values at time t1.
According to the Kirchhoff’s voltage law, we have

\[
\begin{align*}
V_i &= v_{Cr1} + v_{Lr} \\
v_{Cr1} &= v_{Cr2} + v_{Lr}
\end{align*}
\]  

(1)

and the value of \( v_{Cr1} \) is governed by

\[
v_{Cr1}(t-t_0) = V_{in} - (V_{in} - v_{Cr1}(t_0)) \cos(\omega_r (t-t_0))
\]

(2)

where \( \omega_r = \frac{1}{\sqrt{2L_rC_{r1}}} \) is the resonant frequency of \( L_r \) and \( C_r \).

From (2) and considering the maximum of \( v_{Cr1} \) (denoted as \( v_{Cr1\text{max}} \)), we have

\[
v_{Cr1\text{max}} + v_{Cr1}(t_0) = v_{Cr1}(t_0) - v_{Cr1}(t_0) = 2V_{in}
\]

(3)

By differentiating (1), it becomes

\[
\begin{align*}
\frac{dV_{in}}{dt} &= \frac{i_{Cr1}}{C_{r1}} + L_r \frac{d^2i_{Lr}}{dt^2} \\
\frac{dv_{Cr1}}{dt} &= \frac{i_{Cr2}}{C_{r2}} + L_r \frac{d^2i_{Lr}}{dt^2}
\end{align*}
\]

(4)

A very large capacitance is usually employed for the output capacitor \( C_{b1} \). Therefore, \( v_{Cr1} \) can be considered as a constant and its derivative is zero. It also implies that the current flowing through \( C_{r1} \) and \( C_{r2} \) is the same. Hence,

\[
i_{Cr1} = i_{Cr2} = \frac{1}{2}i_{Lr}
\]

(5)

where \( i_{Cr1} \) and \( i_{Cr2} \) are the currents flowing through \( C_{r1} \) and \( C_{r2} \), respectively.

B. Mode II \([t_2-t_3]\)

In Mode II, all the switches \( Q_1 \) and diodes \( D_{a1}, D_{a2} \) are turned off. The voltages \( v_{Cr1} \) and \( v_{Cr2} \), are kept unaltered and the capacitor \( C_{b2} \) are discharged through \( R_L \), supplying the output power.

C. Mode III \([t_3-t_4]\)

In Mode III, the switches \( Q_1 \) and diodes \( D_{b1}, D_{b2} \) are turned on with zero-current. The output capacitor \( C_{b1} \) are charged up by the input voltage \( V_{in} \) and the charges stored in \( C_{r1} \). Similarly, \( C_{b2} \) is charged up by \( V_{in} \) and charges stored in \( C_{r2} \). Both \( v_{Cr1} \) and \( v_{Cr2} \) become minimal at time \( t_3 \).
D. Mode IV \([t=t_3-t_4]\)

The operation at Mode IV is similar to Mode II, where \(v_{Cr1}\) and \(v_{Cr2}\) are kept constant at their minimum values.

The associated circuits for the four operational modes are depicted in Fig. (3).

For each cycle, the average current flowing to the two switching capacitors should be equal to zero. Denoting \(i_{Cr1}^{(1)}\), \(i_{Cr1}^{(3)}\) and \(i_{Lr}^{(1)}\), \(i_{Lr}^{(3)}\) as the current at \(C_{r1}\) and \(L_r\) in Modes I and III, we have

\[
\int_{t_3}^{t_4} i_{Cr1}^{(1)}(t)dt + \int_{t_3}^{t_4} i_{Cr1}^{(3)}(t)dt = \frac{1}{2} \int_{t_3}^{t_4} i_{Lr}^{(1)}(t)dt + \int_{t_3}^{t_4} i_{Lr}^{(3)}(t)dt = 0
\]

(6)

Assuming no power loss and equating the input-output power of the circuit, it can also be derived that:

\[
\frac{V_i}{2} \int_{t_3}^{t_4} i_{Lr}^{(1)}(t)dt - V_o \int_{t_3}^{t_4} i_{Lr}^{(3)}(t)dt = \frac{V_o}{2} \left[- \int_{t_3}^{t_4} i_{Lr}^{(3)}(t)dt \right] 
\]

(7)

Substitute (6) into (7), we have

\[
V_o = 3V_i
\]

(8)

It should be remarked that the relationship between the input-output voltages given in (8) is governed by the circuit topology, i.e. the number of stages designed [15].

3. AUTOMATED SNEAK IDENTIFICATION

The circuit analysis in Section 2.1 presents the desired operational modes of the RSC converter given in Fig. (1).
Recently, it is found in [9-13] that some sneaking operational modes may exist in power converter circuits, affecting their performance. In the followings, a scheme for identifying these sneaking operational modes is described.

### 3.1. Topological States Represented by Boolean Matrix

The on/off stages of switching components, for example the MOSFETs and the diodes in Fig. (1), govern its operational modes. Referring to Fig. (1), the following Boolean matrix can be constructed:

\[
A = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{bmatrix}
\]

(9)

where

1. each column represents the on/off state of a component in the design; the 1st to 6th columns represent the MOSFETs Q1, Q2, and Diodes D1, D2, D3, D4 while the 7th to 13th columns represent \( R_1, \ C_{b1}, C_{r1}, L_r \) and \( V_{in} \) as indicated in Fig. (1);
2. the state of a switching component can be ‘1’ and ‘0’ denoting the state of ‘on’ and ‘off’, respectively;
3. the state of a non-switching components, e.g. capacitors, inductors or resistors, is always ‘1’ (Note: these columns are dummy and can be deleted. They are only included for completeness).
4. each row represents a potential circuit of the power converter

It is obvious that the possible number of states is \( 2^n \) where \( n \) is the number of switching components in the circuit. However, many of them are in fact invalid and the matrix \( A \) in (9) can be reduced to its simplest form.

### 3.2. Qualitative Reasoning and Knowledge

In order to extract the sneaking operational modes, it is required to eliminate all the invalid topologies represented by (9). It can be achieved based on qualitative reasoning and the circuit theory. Referring to the RSC in Fig. (1), the following principles of operations are established:

1. Since the duty cycle of the main switches, \( Q_1 \) and \( Q_2 \), is 50% and they are not allowed to be on or off at the same time, any row with same symbol in the first two columns (i.e. state of \( Q_1 = \) state of \( Q_2 \)) should be eliminated. Particularly, all the switches \( Q \) and diodes \( D_{a1}, D_{b1} \) are turned off which represent Mode II and IV in Fig. (3) should be reserved.
2. To achieve zero-current switching, the circuit must involve both capacitor and inductor. Therefore, using Figs. (1 and 9) as an example, it is an invalid circuit if the following pairs of diodes are both turned on: \( (D_{a1}, \ D_{b1}), (D_{b1}, \ D_{a2}), (D_{a2}, \ D_{b2}) \) or \( (D_{a1}, \ D_{a2}) \).
3. Uni-directional switching devices, i.e. diode in our circuit, with reversed direction cannot be turned on.
4. To obtain the simplest Boolean matrix, a sub-string is considered as a dummy, which can always be deleted. The definition of a sub-string is given in Definition 1.

**Definition 1:** Let \( p = \{ p_i \} \) and \( q = \{ q_i \} \) are two rows in the Boolean matrix, \( q \) is a sub-string of \( p \) if \( q_i \leq p_i, \forall i \).

### 3.3. Sneaking Mode Identification

Based on the description given in Section 3.2, a MATLAB program has been developed to automatically generate the simplest Boolean Matrix and create the circuits. Equation (10) shows the final simplest matrix \( B \) obtained:

\[
B = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 \\
\end{bmatrix}
\]

(10)

As compared with the normal operational modes given in Fig. (3), which can be represented by the following matrix \( B_0 \):

\[
B_0 = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{bmatrix}
\]

(11)

As compared with the normal operational modes given in Fig. (3), which can be represented by the following matrix \( B_0 \):

\[
B_0 = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 1 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{bmatrix}
\]

(11)

It can be concluded that two sneaking operational modes exist which are represented by the matrix \( C \).

\[
C = \begin{bmatrix}
0 & 1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{bmatrix}
\]

(12)

The corresponding circuits are also automatically generated in MATLAB program as depicted in Fig. (4).

### 4. DYNAMICAL ANALYSIS AND OBSERVATIONS

#### 4.1. Analysis of the Sneaking Operation Mode

To further justify the existence of the sneaking operational modes (Modes I’ and III’) in the studied RSC, a detailed circuit analysis is performed.

Referring to the Mode I’ given in Fig. (4a), the inductance current will not go to zero after the normal Mode I. Instead, it will be kept excited in the branches, \( C_{r1} \cdot D_{b1} \cdot C_{r1} \cdot D_{b2} \cdot L_r \) and \( C_{r2} \cdot D_{b2} \cdot C_{r2} \cdot D_{b2} \cdot L_r \). Define \( I_{C_{r1}}^{(t)} \) as the current flowing through \( C_{r1} \), it is derived that

\[
I_{C_{r1}}^{(t)}(t) = \frac{V_{CH} - V_{CM} \sin(\omega t - t_1)}{2Z_r}
\]

(13)
where \( \omega_r = \sqrt{\frac{1}{L_r C_{r1}}} \) and \( Z_r = \sqrt{\frac{L_r}{2C_{r1}}} \).

Similarly, as indicated in the Mode III' shown in Fig. (4b), the inductance current will continuously be excited after the normal Mode III via the branches \( D_{d1}C_{r1}L_r D_{q1} \) and \( C_{r1}D_{d2}C_{r2}L_r D_{q1}' \). Denoting \( i_{Cr1}^{(3)} \) as the current flowing through \( C_{r1} \) in Mode III', it can be obtained that

\[
i_{Cr1}^{(3)}(t) = \frac{-V_{Cr1\min}}{2Z_r} \sin(\omega_r (t - t_s))
\]

(14)

where the voltage at switching capacitor \( C_{r1} \) is

\[
v_{Cr1}(t - t_s) v_{Cr1\min} \cos(\omega_r (t - t_s))
\]

(15)

with

\[
v_{Cr1}(t_s) = v_{Cr1}(t_s) = -v_{Cr1\min}
\]

(16)

Similar to the normal modes, it can also be proved that the currents flowing through the switching capacitors are the same, and hence the relationship (5) holds.

In Modes I' and III', the output power at the load is given as:

\[
\begin{align*}
&\quad -\frac{V_o}{2} \int_{t_1}^{t_4} i_{Lr}^{(1)}(t) dt + \int_{t_3}^{t_4} i_{Lr}^{(3)}(t) dt = \frac{V_o^2}{R_L} T_s \quad (17)
\end{align*}
\]

where \( i_{Lr}^{(1)} \) and \( i_{Lr}^{(3)} \) represent the inductance current in Modes I' and III', respectively, \( T_s \) is the period of one cycle.

Consider the capacitor voltage \( v_{Cr1} \) during \( t_1 \sim t_4 \), the voltage difference is

\[
v_{Cr1\max} - v_{Cr1\min} = -\frac{1}{C_r} \left[ \int_{t_1}^{t_4} i_{Lr}^{(1)}(t) dt + \int_{t_3}^{t_4} i_{Lr}^{(3)}(t) dt \right] \quad (18)
\]

Substitute (17) into (18),

\[
v_{Cr1\max} - v_{Cr1\min} = -\frac{1}{C_r} \left[ \int_{t_1}^{t_4} i_{Lr}^{(1)}(t) dt + \int_{t_3}^{t_4} i_{Lr}^{(3)}(t) dt \right]
\]

(19)

where \( f_s = \frac{1}{T_s} \).

However, from (3) and (16), it is given that
When \( t = t_5 \), the output voltage and power will be reduced, causing the deterioration of the output characteristics.

4.2. Condition of Existence

As shown in Fig. (5), the currents \( i_{L_r}^{(1)} \) and \( i_{L_r}^{(2)} \) in Modes I' and III' are non-zero. From (13) and (14), the conditions for the occurrence of sneaking operational modes can be obtained as:

\[
\begin{align*}
V_{Cr_{1\text{max}}} - V_{Cr_{1\text{min}}} &= 2V_{in} \\
V_{Cr_{1\text{min}}} &= 0
\end{align*}
\] (22)

When \( t = t_0 \),

\[
v_{L_r}(t_0) = V_{in} - v_{Cr_{1}}(t_0) = V_{Cr_{1}} - v_{Cr_{2}}(t_0)
\] (23)

and when \( t = t_1 \),

\[
v_{L_r}(t_1) = V_{Cr_{1}} - v_{Cr_{1}}(t_1) = v_{Cr_{2}} - v_{Cr_{2}}(t_1)
\] (24)

Since

\[
v_{Cr_{1}}(t_4) - v_{Cr_{1}}(t_5) = v_{Cr_{2}}(t_4) - v_{Cr_{2}}(t_5) = \frac{1}{2C_r}\int_{t_4}^{t_5} i_{L_r}(t)\,dt
\] (25)

From (23)-(25), we have

\[
\Delta V = V_{in} - V_{Ch_{1}} = v_{Ch_{1}} - v_{Ch_{2}} = V_a - V_{Ch_{1}}
\] (26)

and

\[
\Delta V = \frac{V_a - V_{in}}{2}
\] (27)

Therefore,

\[
v_{Ch_{1}} = V_{in} + \Delta V = V_{in} + \frac{V_a - V_{in}}{2}
\] (28)

Substitute (28) into (22), the occurrence condition for the sneaking operational modes is

\[
R_s C_{f_s} < 1.5
\] (29)

4.3. Experimental Results

In order to experimentally confirm the analysis given in the previous sections, the RSC converter in Fig. (1) has been built with the components listed in Table I.

An example is given in Fig. (6a) where \( V_{in} = 2V, f_s = 42kHz \) and \( R_s = 22\Omega \). However, when the load drops below the critical value, sneaking operational modes are excited and the resultant output waveforms are obtained as depicted in Fig. (6b). It clearly shows that the results are well matched with the analytical ones. Minor deviation is noticed which is probably due to the internal resistance of power supply and the forward voltage drops in the diodes.
CONCLUSION

In this paper, the existence of sneaking operational modes in soft-switching power converter is reported. They are excited by some undesired topological states, which can be revealed by the construction of a Boolean matrix, representing all the feasible on-off states of the switching components. In particular, a common 3-stage step-up resonant switched capacitor converter has been analyzed. It is mathematically proved that, if certain condition is fulfilled, sneaking operational modes will occur and the dynamics of the power converter are affected. This phenomenon is also confirmed both in simulations and experiments. Finally, it should be remarked that similar analysis can be performed in the designs of other power converters or soft-switching devices, serving as a performance and reliability test.

CONFLICT OF INTEREST

The author confirms that this article content has no conflict of interest.

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