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Carrier Level Layered Modulation Method can Filter Out the Harmonics of Cascaded H - Bridge Topology

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Abstract: Analysis of the reason of cascade H-bridge inverter topology using carrier phase shift modulation method cannot compensate the harmonic, using carrier level layered modulation method can solve the problem of cascade H-bridge topology that it cannot compensate harmonic problems. Experimental results show that the modulation algorithm can effectively reduce the modulation delay, improve the control bandwidth, it can also make the harmonic compensation capacity increase from 5 times to 21. The scope of the application of STATCOM is greatly increased in the grid.

Keywords: Cascade H bridge, carrier level layered modulation, carrier phase-shifting modulation, harmonic compensation, PWM, STATCOM.

1. INTRODUCTION

Cascade H bridge is the mainstream topology structure of the high-voltage power electronic equipment (such as static synchronous compensator STATCOM, large-scale energy storage), which uses H bridge as a unit. Static synchronous compensator STATCOM as shown in Fig. (1) can issue any specified current, improve power quality, support the voltage, suppress voltage flicker, control power flow. H bridge cascaded can withstand high voltage, equipment without transformer and can be straightly hanged in the high voltage power system.

At present, modulation methods of cascade H bridge are as follows: the ladder wave pulse width modulation, multilevel voltage space vector modulation, carrier phase shift modulation [1]. The ladder wave pulse width modulation refers to that the modulation signal use pulse width modulation method for step wave, it filter out harmonic by controlling the length of the conduction time of the maintenance of the single level, particularly for low-order harmonics suppression [2]. Multi-level voltage space vector modulation is a modulation method which is developed on the basis of the two-level voltage space vector modulation [3]. For N-level voltage space vector modulation, in the space of rotating coordinate system, the vector of any time are synthetized by the adjacent N nonzero vector, through the optimization of acting time on the N nonzero vector and zero vector in a modulation period. We can get the output waveform of PWM, its voltage space vector number is N3, because it is a cubic relationship between the number of levels and the number of voltage space vector. When N is large, the

number of multi-level voltage space vector will be too much, causing the control to be more complicated, so the scope of application has been greatly limited [4-6]. Carrier phase shift modulation: control signal for each unit is generated by the phase comparison of a sine modulation wave and two complementary triangular carrier, The modulated wave of the same phase is same, the difference of the carrier is π/N . By controlling the phase shift of the carrier cell output voltage pulse shifted in phase from each other, it can be superimposed to get multi-level waveform [7, 8]. Carrier phase shift modulation control algorithm is simple and easy to implement, and it is also applied to occasions in which N is large, so it is the one that is most widely used as a cascade H-bridge modulation.

Theoretically, STATCOM harmonic compensation capacity, which only depends on the switching frequency. Hbridge IGBT high frequency switching device, the switching frequency can be done to dozens kHZ. It is completely possible to track and compensate for the 50 times harmonic whose frequency is within 1kHZ, but in fact, the current STATCOM can only compensate harmonic near 3, 5 times, as for harmonic more than 5 times, you cannot achieve good compensation effect, it is so far with the theoretical compensation capability. This greatly limits the practical application of STATCOM.

2. THE REASONS OF THE CASE THAT CURRENT STATCOM CANNOT COMPENSATE FOR THE HIGHER HARMONICS

Assuming that the number of cascade H-bridge is n, each carrier of H-bridge is sequentially phase-shifted for 360 / n, and the tangent to the sinusoidal modulation wave can obtain PWM wave, the phase shift modulated carrier is as shown in Fig. (2).

Corresponding PWM wave is as shown in Fig. (3).

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Fig. (1). H-bridge cascade STATCOM.



Fig. (2). Carrier phase modulation in H-bridge cascade (one cycle).

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Fig. (3). Carrier phase PWM wave in H-bridge cascade.

Assuming the input of STATCOM DC-side is Udc, the modulation signal of sine wave is $Us=sin(w1t + \phi)$, thereby the output voltage harmonic component of each unit is as follows.

$$\begin{cases} u_{1n} = \sum_{n=2}^{\infty} \left\{ (-1)^{\frac{n}{2}} \times \frac{4U_{dc}}{n\pi} \times 2\sum_{k=1}^{\infty} J_k (\frac{n\pi M}{2}) \sin(k(\omega_i(t + \frac{T_c}{4}) + \varphi)) \cos(n\omega_c t) \right\} \\ u_{2n} = \sum_{n=2}^{\infty} \left\{ (-1)^{\frac{n}{2}} \times \frac{4U_{dc}}{n\pi} \times 2\sum_{k=1}^{\infty} J_k (\frac{n\pi M}{2}) \sin(k(\omega_i(t + \frac{T_c}{4}) + \varphi)) \cos(n(\omega_c t + \frac{1}{N}\pi)) \right\} \\ \dots \\ u_{Nn} = \sum_{n=2}^{\infty} \left\{ (-1)^{\frac{n}{2}} \times \frac{4U_{dc}}{n\pi} \times 2\sum_{k=1}^{\infty} J_k (\frac{n\pi M}{2}) \sin(k(\omega_i(t + \frac{T_c}{4}) + \varphi)) \cos(n(\omega_c t + \frac{N-1}{N}\pi)) \right\} \\ (n = 2, 4, 6, \dots; k = 1, 3, 5 \dots) \end{cases}$$

$$J_n(x) = \sum_{m=1}^{\infty} (-1)^m \frac{x^{n+2m}}{2^{n+2m} \cdot m! \cdot (n+m)!}$$

Jn is a k-order Bessel function.

The harmonic voltage in total voltage of Cascade Hbridge's output can be obtained as follows.

$$u_{n} = u_{1n} + u_{2n} + \dots + u_{Nn}$$

= $\sum_{m=1}^{\infty} \left\{ (-1)^{mN} \times \frac{2U_{dc}}{m\pi} \times \sum_{k=1}^{\infty} J_{k}(mNM\pi) \sin((k\omega_{1} \pm 2mN\omega_{c})t + k(\omega_{1}\frac{T_{c}}{4} + \varphi)) \right\}$
(n = 2,4,6,...;k = 1,3,5...)



Fig. (4). Double loop control used by STATCOM.

Thus the output voltage harmonic mainly distributed in the vicinity of 2mN times of the carrier frequency wc, and shows odd distribution. The harmonic amplitude increases with the increase of the modulation depth M.

The delay of PWM is half of carrier cycle, assuming that the frequency of carrier is F, the delay of modulation is 1/2F, that is to say the pure delay time is

$$\tau_0 = 1/2F$$
, the delay link is

$$G(s) = e^{-\tau_0 s} = \frac{1}{e^{\tau_0 s}}$$

In China, 10kV STATCOM usually use 12 H-bridge cascade, assuming that the equivalent switching frequency is 21.6kHZ, using a carrier phase shift modulation, the switching frequency of each level is

$$\frac{21.6k}{12} = 1.8kHz$$

The time constant of this delay link is

$$\tau_0 = \frac{1}{(2 \times 1.8k)} = \frac{1}{(3.6k)}$$

The impact on bicyclic control is as shown in Fig. (4).

Vref is the voltage reference value of BUS capacitor in H Bridge, Iref is the reference value of the harmonic needs to be compensated or reactive current. Control algorithm uses double loop of voltage control loop and current loop. Gif(s) and Gvf(s) is the controlled object of current loop and voltage loop. Gi(s) and Gv(s) is the correction ring of the current loop and voltage loop. G(s) is a pure delay caused by the modulation links.

Whether by any modulation, pure delay caused modulation are half cycle of PWM carrier. So in practical applications of power electronics, the current loop control bandwidth is generally designed to be about one tenth of the PWM switching frequency, modulation delay can be ignored. The control loop can achieve the ideal tracking results [9, 10]. Assuming that the equivalent switching frequency is 21.6k, current loop bandwidth is designed to be 21.6k / 10 = 2160Hz. The grid fundamental frequency is 50HZ, that is, in theory, the device can track and compensate harmonics within 2160/50 = 43 times.

But because the H bridge cascade is using the modulation of carrier phase shift modulation, so the modulation delay is not $1/(2 \times 21.6k)$, but to be $\tau_0=1/(2 \times 1.8k)$. In other words: PWM modulation delay time is much larger than the equivalent PWM switching time [11, 12]. So as to achieve stable and accurate tracking current reference given requirements, the control bandwidth of current loop can be designed only up to a maximum of 1.8k/10=180Hz or so, instead of 21.6k/10=1260Hz. Modulation uses the method of carrier phase shift, STATCOM can only compensate harmonics within 3,5 times. STATCOM that use of the carrier phase shift modulation can track and compensate low-order harmonics effectively that within five times. It is mainly used to compensate reactive power and issue reactive power to adjust the voltage.

3. THE INNOVATION OF CARRIER LEVEL LAY-ERED MODULATION

The modulation effect of time delay on cascaded H bridges cannot be ignored, so this paper carries on the transformation to the PWM modulation: For the carrier, X axis represents phase, Y axis represents the level. Since that the modulation method of making sharing of the phase in the X-axis will cause delay modulation that cannot be ignored, so we try to make changes in the Y-axis, making sharing of the level [13, 14]. Average amplitude of the carrier is one of the n points of the original amplitude. The carrier frequency is changed to be n times of the original carrier, that is, the equivalent switching frequency. As is shown in Fig. (5).

The principle of generating the PWM wave in every level of the H bridge is still the same. When the modulation wave is higher than the carrier level, the PWM outputs a high level, when the modulation wave is lower than the carrier level, the PWM outputs a low level. The corresponding levels of PWM wave are as in Fig. (6).

When using the method of carrier phase shift modulation, the device switching frequency (J_G) and the carrier frequency (J_C) are the same, and the equivalent switching frequency (J_D) is

$$f_D = (N-1)f_G = (N-1)f_C$$

When using the method of carrier level layered modulation, the equivalent switching frequency and the carrier frequency are the same, that is $J_D=J_C$, so that the average switching frequency of the device is

$$f_G = f_C / (N - 1)$$

Therefore, corresponding to the harmonic analysis formula, in the same equivalent switching frequency, the Wc is more lager when using the method of carrier level layered modulation.



Fig. (5). Carrier level layered modulation (one cycle).

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Fig. (6). Carrier level layered modulation PWM wave

For the two kinds of modulation methods of Fig. (3) and Fig. (6), using the same synthetic method of PWM, the PWM wave contrast chart of the output of H bridge cascaded are as shown in Fig. (7).

As can be seen from Fig. (7), the equivalent switching frequency of the two PWM is the same. In order to facilitate to see the difference between them, add a FIR filter in the back of two cascaded PWM output, we can get the output of two sine waves. Compared with the modulated wave, it is as shown in Fig. (8).

In Fig. (8), the green is the modulation wave, the blue is level stacked carrier modulation, the red is carrier phase shift modulation, Visibly, the output of carrier level cascade modulation and the modulation wave fits well, substantially without errors. While the output of carrier phase shift modulation and the modulation wave has an obvious phase delay. The delay time is half cycle of the carrier wave, and the waveform distort.

In theory, any delays in modulation are half of the carrier cycle [15, 16]. The modulation delay of carrier level layered modulation is half of the carrier cycle, but because the carrier frequency of this modulation is the equivalent switch frequency, is n times of the phase shift modulation (n is the number of cascaded). Therefore, in the carrier level layered

modulation , the delay time caused by modulation delay is $1\!/\!n$ of the latter.

Assuming that the equivalent switching frequency is 21.6k, then the modulation delay of level stacked modulation is

$1/(2 \times 21.6k) = 1/43.2k$

Theoretically, applying level layered modulation can track and compensate harmonic of the upper limit of $43.2k/10/50 \approx 86$ times. In fact, taking switching loss, cost, demand and other factors in reality into account, in the application, we can track and compensate the harmonic within 21 times.

In the field of Cascade H-bridge topology, has not seen any theory and applications of carrier level stacked modulation methods in this field.

4. EXPERIMENTAL VERIFICATION

To verify the validity of stacked carrier level modulation, we applied this modulation method in a 10kV 12 level cascaded H bridges STATCOM, the field device is as shown in Fig. (9).



(a) Output PWM of carrier level H-bridge layered modulation.



(b) Output PWM of carrier level cascade H bridge cascade modulation.

Fig. (7). The PWM output of two kinds of H-bridge cascade modulation.



Fig. (8). The comparison of the output of two modulation methods and modulated wave.



Fig. (9). High voltage STATCOM site.



(a) harmonic currents before compensation.



(b) almost no harmonic current after compensation.

Fig. (10). Three-phase voltage and current waveforms before and after compensating harmonics.



(a) The valid values of current harmonics before compensation is 275A.



(b) The valid values of current harmonics after compensation is 141A.

Fig. (11). The distribution histogram of current harmonic before and after compensation.

Power quality analyzer records the data before and after the harmonic compensation, compensation interval before and after the load fluctuation within a minute can be ignored [17, 18]. Fig. (10) is a comparison chart of three-phase voltages and current before and after harmonics compensation. You can see the current waveform compensated significantly became better, and the amplitude was significantly reduced. Fig. (11) is a comparison of current harmonic distribution histogram before and after compensation. It can be seen from the figure that after compensation, the harmonic amplitude of harmonics within 21 times has significant attenuation. Fig. (12) is a comparison of the current total harmonic distortion rate before and after compensation. It can be seen from the figure that after compensation, the current distortion THDi is reduced from 9.29% to 3.32%. The harmonic compensation effects of 5, 7, 11,13,19 times are obvious. Visibly, this modulation effect is good in actual application. And prior to the adoption of the carrier phase shift modulation, harmonic compensation can only be achieved within five times [19, 20].

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(a)



(b)

Fig. (12). The detected value of current distortion THDi before and after compensation.

CONCLUSION

This article is presented for the first time and to apply the carrier level layered modulation method in the H bridge cascaded topology, it has the same equivalent switching frequency with the carrier phase shift modulation, but the modulation delay shortened to 1 / n (n is the number of cascaded), fundamentally solve the restrictions on current loop controller bandwidth produced by pure delay. The harmonic compensation will range from 5 up to 21 times. Finally, we verified the modulation algorithm proposed through the experiment, the experimental results show the practicality and effectiveness of the algorithm.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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REFERENCES

- [1] L. Jianlin, Carrier Phase Shifted Cascade H Bridge Multilevel Converters and the Study of its Application in Active Power Filter, Zhejiang University: Hangzhou, 2005.
- W. Yi, Research on Novel Topology and Control Strategy of Cas-[2] caded Multilevel Inverter, North China Electric Power University: Baoding, 2005.
- [3] Y. Bo, Research on H Bridge Efficiency Optimization and the Problem of Capacitor Voltage Balance in Chain STATCOM, Xi'an University of Technology: Xi'an, 2014.
- [4] Z. Yun, Asymmetric Hybrid Multilevel Inverter Modulation Strategy Equilibrium and Power Control, Harbin University of Science and Technology: Harbin, 2010.
- Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, [5] "Small signal model based control strategy for balancing individual DC capacitor voltages in cascade multilevel inverter-based STAT-COM", IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2259-2269, 2009.
- J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, [6] and J. M. Carrasco, "Simple unified approach to develop a timedomain modulation strategy for single-phase multilevel converters", IEEE Trans. Ind. Electron., vol. 55, no. 9, pp. 3239-3248, 2008.
- [7] X. She, A. Q. Huang, and G. Wang, "3-D space modulation with voltage balancing capability for a cascaded seven-level converter in a solid-state transformer", IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3778-3789, 2011.
- [8] H. Iman-Eini, J. -L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers", IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2428-2442, 2008
- X. Shukai, S. Qiang, and Z. Yongqiang, "Research on compensa-[9] tion for unbalanced transformer isolation type chain D-STATCOM," In: Proc. CSEE, vol. 26, no. 9, pp. 137-144, 2006.

- [19] D. G. Holmes, "The significance of zero space vector placement for carrier-based PWM schemes", IEEE Trans. Ind, Appl., vol. 32, no. 5, pp. 1122-1129, 1996.
- [20] S. Kouro, J. Rebolledo, and J. Rodríguez, "Reduced switchingfrequency-modulation algorithm for high-power multilevel inverters", IEEE Trans. Ind. Appl., vol. 54, no. 5, pp. 2894-2901, 2007.

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- [10] M. S. A. Dahidah, and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula", IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1620-1630, 2008.
- [11] B. P. McGrath, and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 858-867, 2002.
- R. Naderi, and A. Rahmati, "Phase-shifted carrier PWM technique [12] for general cascaded inverters", IEEE Trans. Power Electron., vol. 23, no. 3, pp. 1257-1269, 2008.
- G. Carrara, S. Gardella, and M. Marchesoni, "A new multilevel [13] PWM method and theoretical analysis", IEEE Trans. Power Electron., vol. 7, no. 3, pp. 497-505, 1992.
- B. Mwinyiwiwa, Z. Wolanski, and Y. Chen, "Multimodular multi-[14] level converters with input/output linearity", IEEE Trans. Ind. Appl., vol. 33, no. 5, pp. 1214-1219, 1997.
- [15] D. G. Holmes, and T. A. Lipo, Pulse Width Modulation for Power Converters: Principles and Practice. Wiley-IEEE Press: America, 2003
- [16] A. Iqbal, and S. Moinuddin, "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI", IEEE Trans. Power Electron., vol. 24, no. 10, pp. 2379-2390, 2009.
- W. Fei, "Sine-triangle versus space-vector modulation for three-[17] level PWM voltage-source inverters", IEEE Trans. Ind. Appl., vol. 38, no. 2, pp. 500-506, 2002.
- N. V. Nho, and M. -J. Youn, "Comprehensive study on space-[18] vector-PWM and carrier-based-PWM correlation in multilevel inverters", IEEE Proc. Electr. Power Appl., vol. 153, no. 1, pp. 149-158.2006.

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