Audio Data Acquisition System Design Based on ARM and DSP

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Abstract: With the rapid development of embedded technology and multimedia technology, the digital audio technology has been widely applied. According to an audio data acquisition system, this paper introduces the communication interface design on the basis of HPI between ARM and DSP, and A/D, D/A converter design, describes the operating principle of interfaces and relevant configuration. A method of audio data acquisition is presented, control is based on ARM, DSP takes charge of signal processing, it provides the system chart of data acquisition and software flow chart. This design scheme can take full advantage of McASP interface to achieve high-precision AD & DA converter, and HPI interface is used to realize high speed data transfer between ARM and DSP, thereby achieving efficient and real-time transmission of huge amounts of audio data stream.

Keywords: HPI (host port interface), DSP, ARM, Data acquisition.

1. INTRODUCTION

In the field of audio applications, a large number of operations are often needed on audio data such as acquisition, processing, transmission, storage and other operations at the same time. Only adopt DSP and ARM processor cannot meet the system requirements of real-time and high efficiency, so the combination of ARMS and DSP are used by more and more embedded real-time application systems to achieve higher performance. Among them, the ARM is as the main processor, which is responsible for the task management, interface control, human-computer interaction; And as the dependent processor, DSP is responsible for data processing [1]. In the high speed data acquisition system very consist of ARMS+DSP, the rate of data transmission between ARM and DSP determines the whole performance of the embedded system. Based on fast audio data acquisition system as an example, this paper introduces the data acquisition system design plan of ARM and DSP based on HPI interface, the hardware design method and the software flow chart of data acquisition system are also given

2. THE WHOLE STRUCTURE OF SYSTEM

The S3C2440 micro controller of the ARM9 series of Samsung is adopt as the ARM processor of this system which is based on the ARM920T processor, has the Harvard structure, the independent 16 KB instruction Cache and data Cache, and has an abundant system resources, the clock frequency of it can be up to 400 MHz [2]. It is suitable for the applications of patterns sensitive on cost and power. The 32-bit high speed floating point TMS320C6713 chip of TI Company as the DSP, the maximum frequency of clock is 300 MHz [3]. The single instruction execution cycle of it is only 5 ns, the processing speed is fast, and it has powerful operation ability with the calculation speed up to 2400 MIPS/1800 MFLOPS [4]. Mainly used for high performance signal processing occasions, the chip can meet the demands of audio algorithm of data processing.

The main functions of the system is based on 96 kHz/24 bit high precision sampling rate real-time acquisition of voice signal, DSP frequency interpolation, digital filtering, effect after processing, real-time playback by D/A conversion. DSP processing of data and the result was using the HPI interface, through ARM transmitted to PC through USB or Ethernet for data analysis, to understand the working state of the audio signal of the current, and the results are analysis and research to achieve high fidelity quality management. System is mainly composed of A/D conversion unit, data processing unit, the host communication unit, D/A conversion unit and power supply module, the structure diagram is shown in Fig. (1).

3. INTERFACE DESIGNS OF S3C2440 AND TMS320C6713

In the data acquisition system, ARM as the main processor is mainly responsible for the communication control, operating system, calling interface driver, and it can also be used as the storage of a mass of audio data. As the dependent processor, DSP is responsible for the A/D sampling and signal processing and D/A conversion. The communication interfaces between ARM and DSP mainly are dual ports RAM, serial interface or host interface HPI. The front two ports require for additional hardware support, and the HPI methods don't need to increase peripheral logic circuit, reduce the hardware cost, is very suitable for occasions that require for high real-time and large quantities of data transmission [5].
Table 1. Description of HPI interface.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD[15:1]</td>
<td>Data bus</td>
</tr>
<tr>
<td>HCNTL[1:0]</td>
<td>Access control register</td>
</tr>
<tr>
<td>HHWIL</td>
<td>Confirm half word (16bits) input</td>
</tr>
<tr>
<td>HAS</td>
<td>Distinguish address and data to reuse address data bus</td>
</tr>
<tr>
<td>HR/W</td>
<td>Choice control of read/write</td>
</tr>
<tr>
<td>HCS</td>
<td>Chip select signal</td>
</tr>
<tr>
<td>HDSI/HDS2</td>
<td>Input data gating</td>
</tr>
<tr>
<td>HRDY</td>
<td>Ready signal</td>
</tr>
<tr>
<td>HINT</td>
<td>Interrupt signal to host</td>
</tr>
<tr>
<td>HWOB</td>
<td>Half word order</td>
</tr>
</tbody>
</table>

3.1 Introduction on the HPI Interface

The HPI (host port interface) is the 16/32 bit parallel interface specifically signed by TI company to meet the DSP and other microprocessor interface communication, external host has the control right of the interface. The interface HPI of TMS320C6713 is a 16-bit parallel port, the ARM can be direct access to the DSP’s internal storage space or address is mapped to the storage space of peripherals through the interface, and it can achieve DSP resources exchange [6].

HPI of TMS320C6713 completes the external communication between the host and DSP through three 32-bit registers as the data registers HPID, the address register HPIA and the control registers HPIC. The HPI interface signal is described in Table 1. External host and DSP can access HPIC, but only the external host can access HPIA and HPID.

3.2 ARM Core Board

The core board is the control and data interaction center of each unit module. This design uses ARM and modules of DSP core boards directly, which is very convenient and saves cost and time. ARM and DSP core board adopts multi-layer system boards, different types are layered set, which increases the anti-interference ability, reduces common-mode interference, and has high stability. Main pins of two core boards are plugged on the floor in the form of pin, convenient circuit development and debugging.

The ARM core board is composed of the following sections:

CPU: The top is adopted with S3C2440A processor encapsulated with FBGA;

Storage: Two pieces of 32M SDRAM, and there is one piece of 64M or 128 M flash extension spaces;

Clock source: Provide 12M system external clock source, 32.768 K RTC clock source;

Power supply: The kernel 1.2V regulated power supply, with the register of voltage regulator module 3.3V.

The core board supports 3.3V and 5V power supply. The bottom is a Samsung 128 MB NAND Flash.

Two pieces of 32M SDARAM consist the 64 MB memory space, when the system is after the charging operation, Boot loader copy mirror image document into the corresponding address space of SDARAM, in this way, an operating system boot software platform is set up.

3.3. The Design of ARM and DSP Interface

ARM micro controller (S3C244) as the main controller, its external I/O achieve the shake hands and interrupt request ARM and DSP software for three registers (HPIA, HPIC and HPID) of the HPI interface respectively, latch ARM from accessing DSP storage unit address, and exchange data. Namely that ARM access the whole storage space of DSP through addressing the HPI three registers and conduct the
shake hands communication of DSP. The hardware connection of S3C2440A with TMS320C6713 is shown in Fig. (2).

The host operates and chooses to access the HPI registers through HCNTL0 and HCNTL1 these two signal lines, (as shown in Table 2). HCNTL1 and HCNTL0 of HPI are connected respectively to the S3C2440 address line ADDR2 and ADDR1, different registers can be visited through the operation on ADDR [2:1]. HR/W read/write the input signal for the HPI, when the host drive HR/W=1, the HPI can be carried on the read operation; Otherwise, writing operation of HPI is conducted [7]. As there is no read/write gating signal of S3C244, so ADDR4 is chosen to join the HR/W, control the reading and writing states of the HPI through the operation on this address line. HHWII and S3C244 of TMS320C6713 are connected to ADDR3, which are used to identify whether it is the first half word or second half a word in the transmission, when ADDR3 is zero, it shows the read and write of first half word, and when the ADDR3 is one, it shows the read and write of the second half word, and which bytes is the high half word is determined by the HPIC HWOB [8].

HCS is the Chip Select signal of HPI, which is connected with selected signal of host nGCS4. The data gating signal is common made up of HCS, HDS1 and HDS2; the signal is the operation results of the xor between HDS1 and HDS2 and the nand operation with HAS after that. HAS is the gating signal address, due to the S3C244 having independent address and data bus, HAS high level can be fixed. HRDY is connected to the nEWAIT pin of the host, to indicate the current state of the ready HPI access. HINT interrupt signals are picked up to the external I/O ports on EINT3 of S3C244. HINT is the interruption application that DSP send to host, and ARM of the host triggers the interrupt of DSP by setting the DSPINT bit in HPIC. By the DSPINT and HINT bits in the HPIC register, the interruption can be sent between ARM and DSP, to coordinate the communication between ARM and DSP.

### Table 2. Operation choice of HPI register.

<table>
<thead>
<tr>
<th>HCNTL0</th>
<th>HCNTL1</th>
<th>Function Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Host can read and write HPIC.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Host can read and write HPID, HPIA increase by one after each read operation or decrease by one after each writing operation.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Host can read and write the HPIA, this register aim at HPI storage.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Host can read and write HPID, thus HPIA wouldn’t be affected</td>
</tr>
</tbody>
</table>

Fig. (2). Data acquisition system structure.
y(n) = \sum_{i=0}^{N-1} a_i x(n-i) \quad (1)

The general form of it is (h(i) is impulse response):

y(n) = \sum_{i=0}^{N-1} h(i)x(n-i) \quad (2)

After Z exchange, the system function H(z) of FIR filter can be obtained from the upper formula

H(Z) = \sum_{i=0}^{N-1} h(i)z^{-1} \quad (3)

4. INTRODUCTION OF MCASP INTERFACE

4.1. Overview of McASP

McASP (Multichannel Audio Serial Port) takes the form of time division multiplexing data streams. MCASP use 12S agreement, and also support D1T protocol. It has convenient interface audio equipment to send and receive master clock (AHCLKX, AHCLKR) and mute control (AMUTEIN AMUTE), the serial data lines of MCASP are up to eight roots. Two multichannel audio serials MCASPO and McASP1 are integrated on C6713, these two MCASP reuse external pins with other peripherals on a chip module.

4.2. McASP Characteristics

McASP is the specific audio access interface on DSP of TI Company. It has the following features:

1) Send and receive independent clock;
2) The sending and receiving modules include: Programmable clock and frame synchronization signal generator; 2, 32, 384 of slot TDM data flow; slot which supports 8, 12, 16, 20, 24, 28 bits; the data format bit operation;
3) A total of 16 serial data pins;
4) Can be seamless connected with audio codec, DIR;
5) Compatible with S agreement and supports I2S data format;
6) Integrate the digital audio interface transmitters;
7) When used as DIR receiver, external digital audio interface receiver can be used as the conversion of IIS data format;
8) Error checking and correction

5. INTERFACE DESIGN OF A/D AND D/A

McASP (multichannel audio serial port), is a multi-functional synchronous serial interface which is convenient for interface multichannel audio equipment on the 6713 microprocessor. McASP can be configured to a variety of synchronous serial interface standards, which can be directly connected with high-speed interface of all kinds device. McASP can send and receive two separate clock generators, and the send and receive can be adopted in different clock frequency; There are total 16 serial data pins; seamless connection can be achieved between McASP and audio ADC, DAC, Codec, digital audio interface receiver DIR and transmission physical device S/PDIF; Multiple IIS data types, and similar data formats can be supported.

DFS is the selection signal of data format, THE relationship among LRCK, SCLK and SDATA are controlled by DFS pins, in this system, DFS is set high, and serial data output format should be set at the I\(^2\)S format. S/M is set high, and is configured at the department pattern; LRCK and SCLK are as the input. Chip Select is set high as the I\(^2\)C interface. MCLKA and MCLKD are respectively as the simulating alternative selection input clock and digital selection input clock, the required frequencies of MCLKA/MCLKD are determined by the output sampling rate.

5.1. A/D part

AD chips adopt CS5396 of CRYSTAL Company, CS5396 uses technology, which can achieve 24 bits high-resolution, and support 96 kHz high sampling rate, and the dynamic range is as high as 120dB. Its input adopts differential structure in order to eliminate noise jamming of common-mode. Data acquisition system composed by CS5396 has the characteristics of high resolution, wide dynamic range, high signal to noise ratio, etc. which are especially suitable for the occasion of this system that needs high precision data acquisition.

The system has two analog input channels, with a piece of CS5396 to implement, working in a controlled way. The work mode can be set up through A/D control ports by TMS320C6713 (sampling rate, master/slave mode, selection of data format, high-pass filtering forbidden, etc.).

5.2. D/A Part

D/A chip are adopted with WM8741 in Wolfson Company. WM8741 is a stereo DAC with very high performance, which is designed for professional recording system, A/V receiver and the audio application of high-profile CD, DVD and home theater systems.

The length of PCM data input words supported by the device from 16 to 32 bits, the sampling rate is as high as 192 kHz. Signal-to-noise ratio is as high as 128 dB, and distortion degree is 100 dB, which is a high-performance stereo D/A converter, the high precision digital filter can be directly opened under hardware mode, five kinds of digital filters that can response characteristics are set inside, three of which are opened under hardware mode, and other two controlled by software, which is very suitable for this design.

WM8741 set the control mode of hardware that is to pull or drop-down situation to determine the working state through specific pins, and all the resistance of the pull or drop-down are 10kΩ. Settings of WM8741 control pins are shown in Table 3.
5.3. The Design of PCB

The design of PCB (printed circuit board) starts from the principle diagram, the whole design process is done according to the principle diagram; the circuit design tools are Protel DXP 2004 of Altium Company. The correctness and completeness need to be paid attention to during the design process of the principle diagram, the label, ports, and the ensure of the connection cables, network bus on electrical connection should be confirmed correctly, the connection of cross line must be placed by Junction (nodes) to build. Schematic diagram should be clear to read, network label of each unit circuit can be used as more as possible. In the process of PCB design, the summarization is as follows:

1) The Layout of the Components

Roughly structure should be planned at first, such as peripheral interface circuit, serial interface circuit, the general location of the CODEC circuit etc., such as ARM and DSP circuit are respectively around in two parts, leading out the HPI interface cable in the middle. In this principle, the edge of the PCB components should be more than 2mm from plate edge.

Considering the fixed position of components, place the closely related to the structure components from the angle of structure design, such as sockets, switches, indicator lights, fittings and so on, the LOCK function of the software had better be used to lock its position, to avoid the mistaken replacement. Then the core components, special components and big components should be placed. Finally the small devices such as resistors, diodes, auxiliary small IC should be placed, according to which unit circuit it is affiliated to in the position, function and role of principle diagram, the layout of its core components is taken to ensure the rationality of the layout, the flow of signal, according to flow to the arrangement of unit function circuit also need to consider, to keep signal fluency.

Electrolytic capacitor shouldn't be too close from the heat source, in order to avoid premature aging of electrolyte and influence its life. Potentiometer, toggle switch, which is convenient for adjustment, such as the adjustment inside machine or chassis panel should be considered in place.

Reasonable distinction between analog and digital parts should be taken, to reduce the interference of signal disaster and electromagnetic. Noise components such as relay should be far away from the sensitive IC. The layout of the components should not only be uniform and reasonable, but the beautiful fluency of the following set should be more considered.

2) Wiring Components

Because the double panel line is used, the two sides of the wires should be perpendicular or oblique, to avoid running parallel to the line, and to reduce parasitic FGC. Walk line corner should be more than 90 degrees as far as possible, it is best to avoid right Angle corner. As the address line or cable, line length difference is not too big. The attachment of signal, components should be as short as possible; its length should not be more than 2cm. Finally welding, commissioning, maintenance convenience should also need to be considered to for the relevant test points for debugging. The ground parts, digital and analog parts should be separated. Low frequency of the circuit should be adapted to single point grounding in parallel; High frequency part, in accordance with the principle of grounding to the nearest should be connected to multipoint ground. If the ground is thin, the grounding potential changes over current, and lowers the antinomies performance. So the ground should be wide and short as far as possible, so it can be set up according to the actual situation or copper need to be set, to improve the location problem.

When the layout of line is finished at last of the text, individual components, layout of line should be adjusted, to check device packaging, DRC, etc., the design of whole board PCB can be finally completed.

6. THE SOFTWARE DESIGN

The main functions of the software design are to complete data collection, read the data into storage, analysis and process data and output data [9, 10]. The software process: start the DSP initialization program, input analog signal to the A/D converter; Start the A/D converter, send interrupt request signal to DSP after finishing the conversion, turn to

### Table 3. Set of WM8741 control pins.

<table>
<thead>
<tr>
<th>Name of Pin</th>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE/LRSEL</td>
<td>Pull down</td>
<td>Hardware control module</td>
</tr>
<tr>
<td>DIFFHW</td>
<td>Pull down</td>
<td>Hardware control module</td>
</tr>
<tr>
<td>OSR/DSDR</td>
<td>High Resistance</td>
<td>96kHz sampling rate state</td>
</tr>
<tr>
<td>SCLK/DSD</td>
<td>Pull down</td>
<td>Input is set as the PCM format</td>
</tr>
<tr>
<td>DEEMPH</td>
<td>Pull down</td>
<td>Forbidden wiping out strengthen function</td>
</tr>
<tr>
<td>IWO/DOUT</td>
<td>Pull up</td>
<td>24 bits I'S interface set in input end</td>
</tr>
<tr>
<td>CSB/SADDR/’S</td>
<td>Pull up</td>
<td>24 bits I’S interface set in input end</td>
</tr>
</tbody>
</table>
the interrupt service subroutine, read data, analysis and process data; the signals after processing are sent to the D/A converter, to realize real time audio playback. Software flow chart is shown in Fig. (3).

CONCLUSION

Features presented in this paper are implementing transmission massive audio data stream through using the HPI interface by controlling ARM, audio data can be read from external audio and sent to the DSP, or the data through the processing of DSP is sent to ARM through HPI interface. The design of the communication of ARM and DSP based on HPI interface, as well as the design of 6713 McASP audio interface with AD, DA interface. This training method can be applied to data acquisition system based on ARM and DSP, which has very good practical values. The data acquisition system adopts TMS320C6713 of TI as the core processor, the S3C2440 of SAMSUNG as the main controller, the TLU320AIC23B of TI as the audio codec, the system design of double CPU mode makes full use of the fast and efficient calculation speed of DSP and the strong control and human-computer interaction ability of ARM. The HPI interface interconnection is used between DSP and ARM to implement the data exchange between dual-core, the audio acquisition and playback are used to realize TLU320AIC23B technique. A complete set of audio data acquisition system is set up, and a basic platform for the acquisition and processing of the real time audio signal is set up.

CONFLICT OF INTEREST

The authors confirm that this article content has no conflicts of interest.

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Declared none.

REFERENCES