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# On Improving the Time Synchronization Precision in the Electric Power System

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**Abstract:** In order to improve the time synchronization precision in the electronic power system, the transmission of the timing information is demodulated based on FPGA. Based on the time service accuracy, the transmission timing information adopts IRIG-B code, the digital Costas loop is introduced in the process of FPGA demodulating IRIG-B code, which can extract the zero-crossing point information of IRIG-B code to avoid the problems of zero drift and pulse jitter in zero-crossing detection circuit. In this article, the time unifying terminal equipment has adopted the BeiDou satellite navigation receiver as the clock source and the output standard is IRIG-B code. The simulation results show that the algorithm reduces the synchronization errors of IRIG-B code, improves the timing synchronization precision, and fulfills the requirement of timing accuracy in the power system.

**Keywords:** IRIG-B, FPGA, time synchronization, timing precision, FPGA.

## 1. INTRODUCTION

Based on the time service requirements in the field of electronic power system, in the power grid of China, the time signal received by the receiving unit of time signals, obtains 1 PPS (pulse per second) and the time message includes the Beijing time and date information as well. The time deviation is less than or equal to 1μs between the leading edge of 1 PPS and the UTC (Universal Time Coordinated) second; 1 PPS and the time message are taken as external benchmark time for the main clock [1].

In the unified device for terminal time, the time information decoding needs to convert the sine wave into a rectangular wave, and performs the zero-crossing detection. In the process of waveform transformation, the zero-crossing detection circuit is usually near zero point and produces jitter and drift due to the channel distortion, unstable signal, and other factors such as noise, which will cause the zero point misjudgment and lower output time precision [2-3]. Based on the method of parallel processing data [4] of programmable logic device (FPGA), this paper adopts FPGA to decode IRIG-B code. The all-digital Costas loop is introduced in the decoding, which is able to extract the zero-crossing information of IRIG-B code to output 1 PPS and time message, as a result the time synchronization precision is improved.

## 2. IRIG-B CODE TIMING SYSTEM

BeiDou (COMPASS) satellite navigation system (the second generation BeiDou) is a global satellite navigation system with independent development and independent operation that China is implementing. It is made of 5 geostationary orbit satellites and 30 non-stationary orbit satellites. The space satellite's mission is to complete the forwarding of two-way radio signals between center control system and user transceiver. There are 16 satellites which have been launched successfully in the BeiDou system, covering the entire Asia-pacific region. The open service of BeiDou global navigation satellite system is to provide free positioning services, velocity measurement and timing services, the positioning accuracy is 10 m, the timing accuracy is 50 ns, and the speed measuring precision is 0.2m/s [5-6].

According to the development and the timing accuracy requirements in the field of electric power system, in this article the time unifying terminal equipment adopts the BeiDou satellite navigation receiver as a clock source, the output standard is IRIG-B code. IRIG-B code is combining the advantages of both the time message with serial port timing and the prospective clock edge, with data pulse timing, to transmit time information. This method only needs to transmit a set of signals, and saves the master clock system resources [7]. In terminal system design, FPGA is used to perform decoding on IRIG-B, the block diagram of demodulation system is shown in Fig. (**1**).

IRIG-B format time code is the time code operating at one frame per second, and the waveform of B (DC) code is shown in Fig. (**2**). From Fig. (**2**), IRIG-B code is the time code with pulse width modulation, it operates at one frame per second, and each pulse is called a code element. IRIG-B code is the time format of pulse width modulation. The index counting interval 5 ms and 2 ms represents binary "1" and "0", respectively. The reference code element (PR) "on time" reference point is the leading edge of the reference code element.

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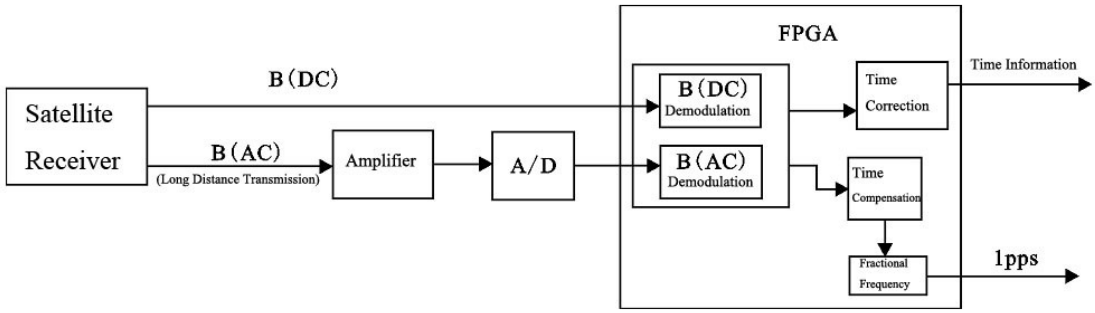


**Fig. (1).** IRIG-B code demodulation system diagram.

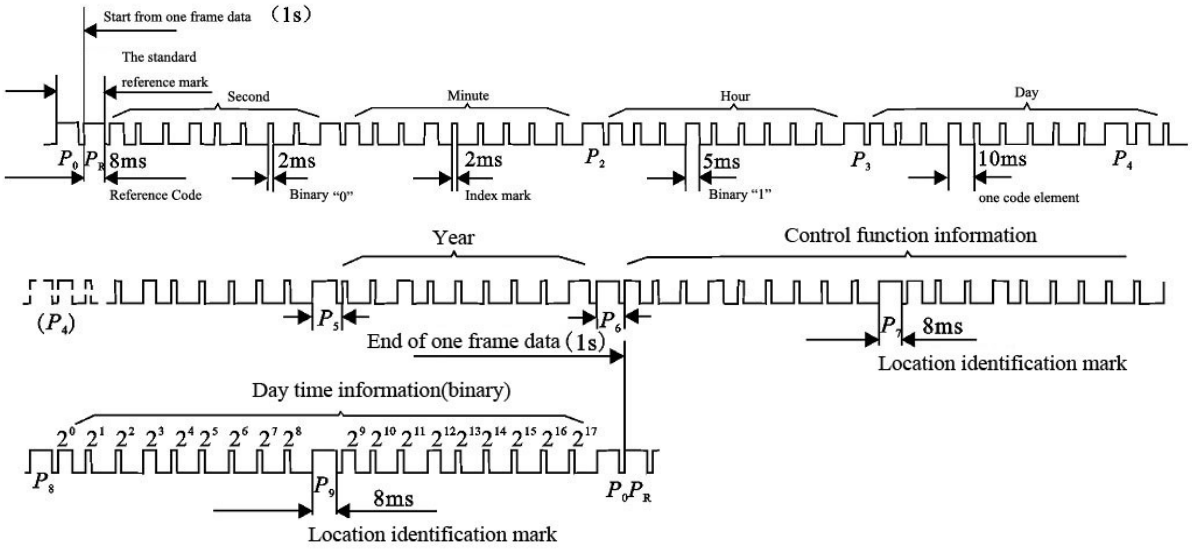


**Fig. (2).** IRIG-B code diagram.

In practice, according to the difference between IRIG-B code transmission distances, IRIG-B code has two types which are the non-amplitude modulated DC code and the amplitude modulation AC code. The non-modulation IRIG-B code is a kind of standard TTL level signal which is applicable to the occasions where transmission distances are relatively small, its precision can reach ns levels. For long distance transmission, sinusoidal modulation IRIG-B code timing is used, however it only reaches ms levels of precision [8-10]. In order to achieve the accuracy requirements for timing in the electric power system, FPGA is used to perform IRIG-B (AC) code decoding, its Costas loop method is used for the zero point tracking, the timing precision can reach μs level.

## 3. IMPROVE THE ACCURACY OF THE INTERFACE TERMINAL B

DC B code can use the cable for transmitting within close range, its time precision is high; when the transmission distance reaches 200 m, it still guarantees signal transmission quality with higher accuracy. IRIG-B (AC) is used for long-distance transmission, the transmission distance can reach 500 m, and therefore its application range is more extensive. After the process of modulation and demodulation, the time accuracy of B's (AC) code signal is reduced.

### 3.1. The Improvement of IRIG-B Code Precision

IRIG-B (DC) transmission uses RS-422 standard interface, after the input DC code converts the level, the B code signal of TTL level is obtained. FPGA is used to do IRIG-B (DC) decoding, when the rising edge of every IRIG-B code element arrives, the count is started, when the falling edge reaches, the counting is stopped. The count value is read to determine if it is 2 ms, 5 ms or 8ms, to determine the value of the code element. At the same time six state machines are used to distinguish the second, minute, day, month, and year, according to the code element and judgment of each state. After confirming which state it belongs to it is transferred to its respective state until the completion of the frame data. After the completion of a frame of data, it is converted to serial data and outputted, and at the same time in the place of two 8 ms to work out 1 pps. Using FPGA to do IRIG-B (DC) decoding, several measures are taken to improve the timing and precision of IRIG-B (DC).

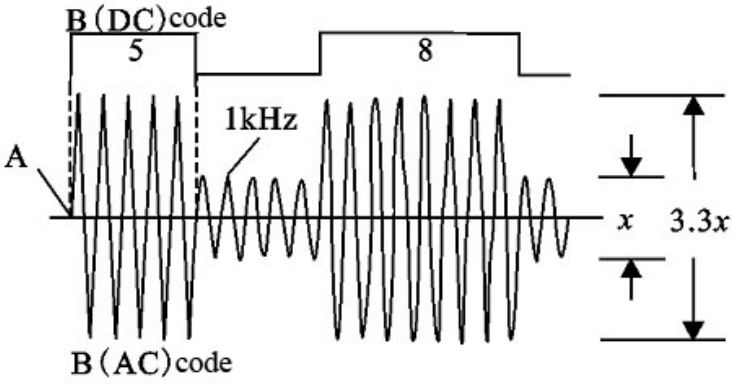


**Fig. (3).** IRIG-B (AC) code modulation schemes.

(1) Increase the external clock frequency

External clock frequency increases one time, the precision will also correspond one time. This method is the most straightforward way, but it is not applied at any given time. This method can improve the decoding accuracy of IRIG-B (DC), but at the same time it also increases the power consumption of the whole system, and because the board running rate is limited, the external clock frequency cannot also be increased.

(2) Adopt the pulse width fault-tolerant technology

Through software or hardware, 1, 2, and 3 ms pulses are discriminated as 2 ms pulse, 4, 5 and 6 ms pulses are discriminated as 5 ms pulse, and 7, 8, and 9 ms pulses are discriminant as 8 ms pulse. Pulse width is discriminated as a fault tolerance.

(3) Strict synchronization and out-of-step criterions

In the decoding, if, within consecutive 3 ms, the data is correct, then the synchronization is allowed. At the same time, if, within consecutive 3 ms. the data is judged as incorrect, it is judged as out-of-step. This process is performed to overcome the error code in the largest extent.

(4) Reduce the 1 PPS pulse width

In the design 1 PPS signal is selected to synchronize each signal for encoding, after the rising edge of 1 PPS pulse is reached, each counter in the chips are reset and the count restarted. But as a result the 1 PPS pulse width is larger, if it is used to perform the reset of the signal directly, there will be a larger error. Therefore, adjusting the pulse width and using the adjusted pulse can improve the accuracy of coding.

To facilitate the transfer of standard time format code, an amplitude modulation on the standard sine wave carrier frequency can be performed. The standard sine signal must be as the same signal source, DC B code, to keep the time relationship constant between them. The standard sine wave carrier frequency is strictly related with the rate of code element, usually it is 10 times that of the code element rate. The standard sine wave frequency of B code is 1 KHZ. At the same time, the orthogonal zero-crossing point (A point in the figure) is corresponding with the front edge of the modulation format code element, the standard modulation ratio is 10:3, and IRIG-B (AC) code modulation diagram is shown in Fig. (**3**).

Because of the noise and distortion caused by signal channel, IRIG-B (AC) code produces jitter and zero point drift after passing the time benchmark pulse of zero-crossing detection circuit, the noise is passed to the output side, which leads to jitters of output time signal [2]. In the decoding of B code (AC) a full digital phase-locked loop is introduced, the loop tracks through the input B (AC) code to obtain the carriers with same frequency and same phase, which also precisely obtains the zero-crossing information carried by B (AC) code. This method overcomes the disadvantages of the zero-crossing detection circuit in the previous demodulation methods. The demodulation principle diagram of IRIG-B code (AC) is shown in Fig. (**4**).

When IRIG-B (AC) signal is demodulated, the synchronization carrier signal must be restored. Currently the methods used in synchronous carrier recovery usually have two types, one type is when sending the signal at the same time, and also sending pilot signals at an appropriate frequency. This method is rarely used practically. Another type is directly extracting from the received signals, the square transformation method and COSTAS loop method may be used for this purpose. Because while getting the same work performance, the working frequency of COSTAS loop method is half of the working frequency of square transformation method. Therefore, COSTAS loop method is more practical [11-13]. In this paper, digital COSTAS loop method is used to recover the carrier of B (AC) code, which is used as the synchronous clock of IRIG-B (AC) code. The composition principle diagram of COSTAS loop is shown in Fig. (**5**).

The voltage controlled oscillator (VCO) in Costas loop outputs two mutually orthogonal carrier signals. The received input signal s(t) is an input for the two phase discriminators to perform a phase discrimination, respectively with the same phase. An orthogonal carrier signal, through a low-pass filter (LPF) outputs band signals, excluding the doubling frequency items, and then multiply to get the error signals, which are sent into the loop filter (LF) to output the control voltage associated with phase difference to control the output of the local carrier source [6].

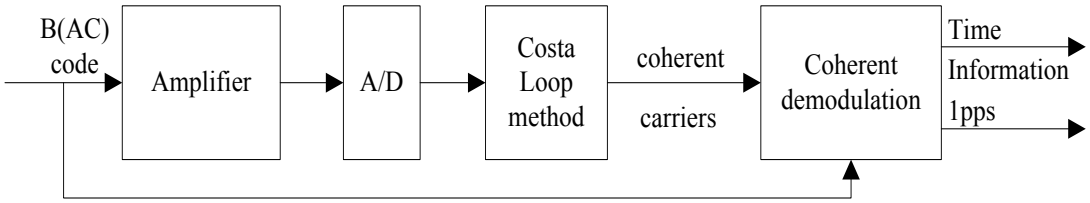


**Fig. (4).** IRIG-B (AC) code demodulation principle diagram.

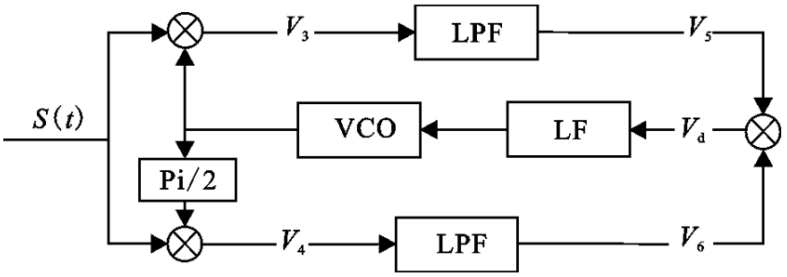


**Fig. (5).** The principle diagram of all-digital COSTAS loop.

Assume that the input signal is

$s(t) = m(t)\cos(w_c t + \theta)$, in the expression, is the modulation signal; is the input signal angular frequency; θ is the initial phase for the input signal. The two-way carrier signals output from local VCO are:

$$\begin{cases} I(t) = cos(w_c t + \varphi) \\ Q(t) = \sin(w_c t + \varphi) \end{cases} \quad (1)$$

In the expressions, $\varphi$ is the phase value of carrier frequency signal that VCO outputs.

After two-way orthogonal signals of the input signal and the local carrier frequency multiply and double the frequency, two-way signals are obtained and shown in the following:

$$\begin{aligned} v_3 &= m(t)\cos(w_c t + \theta)\cos(w_c t + \varphi) \\ &= (1/2)m(t)\left[\cos(2w_c t + (\theta + f)) + \cos(\theta - \varphi)\right] \end{aligned} \quad (2)$$

$$\begin{aligned} v_4 &= m(t)\cos(w_c t + \theta)\cos(w_c t + \varphi) \\ &= (1/2)m(t)\left[\sin(2w_c t + (\theta + f)) + \sin(\theta - \varphi)\right] \end{aligned} \quad (3)$$

After the filtering of low pass filter to remove multiple frequency items, the input expressions of phase discriminator are obtained:

$$v_5 = (1/2)m(t)\cos(\theta - \phi) \quad (4)$$

$$v_6 = (1/2)m(t)\sin(\theta - \phi) \quad (5)$$

After two-way signals pass phase discrimination and multiply, the error control signal is obtained on the loop filter:

$$v_d = (1/8)m(t)\sin(2(\theta - \phi)) \quad (6)$$

When, $\theta$-$\phi$ is always less than 1 radian, $\sin(\theta\text{-}\phi) \approx (\theta\text{-}\phi)$, the error signal is a signal related to phase difference, and eventually the steady-state phase error is reduced to a small value, and there is no residual frequency offset. When the loop is locked, $v_5 \approx (1/2)m(t)$. In the end, the carrier signal output from VCO is the carrier signal required by the system. c1 and c2 are gain factors of two branches in Costas loop filter, the relative value calculation formula is:

$$c_1 = 2\xi w_n T / K_d \quad (7)$$

$$c_2 = (w_n T)^2 / K_d$$

In the expression, $\xi$ is the loop damping coefficient (in engineering generally it is 0.707); $w_n$ is the loop damping oscillation frequency, and $w_n = 8\xi B_l / (4\xi^2 + 1)$; BL is the loop equivalent noise broadband; T is the loop update time; $K_d$ is the overall loop gain.

### 3.2. Data Simulation

In the design of Costas loop, at first the problem is to handle the loop clock. In B (AC) code demodulation, AD module samples at a rate of about 8 KHZ to B (AC) code input signal. The carrier frequency of B (AC) code is 1 KHZ, namely a cycle sampling eight points. If loop noise equivalent width is taken 15 Hz, the loop update time is 1 ms. The working clock of FIR low-pass filter is 8 KHZ, the local accumulation clock of NCO is 8 KHZ, the output carrier frequency is 1 KHZ. The loop parameters are $c1 = 0.022013$,

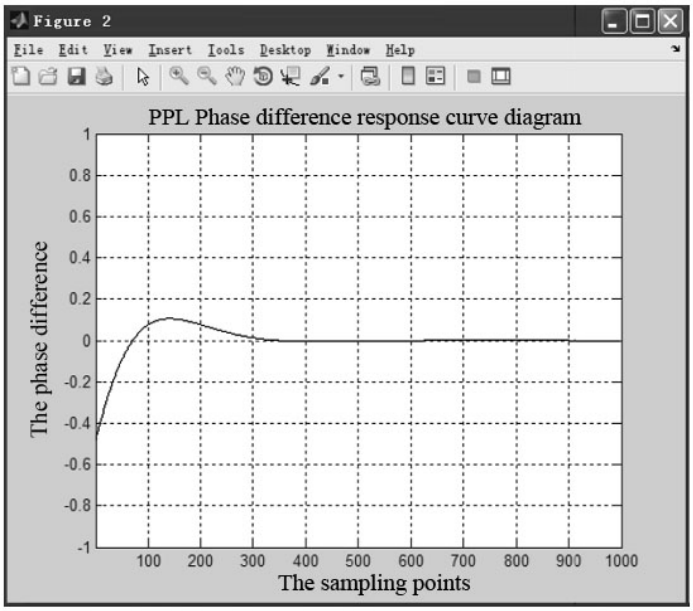


**Fig. (6).** The phase difference between output and input signals.

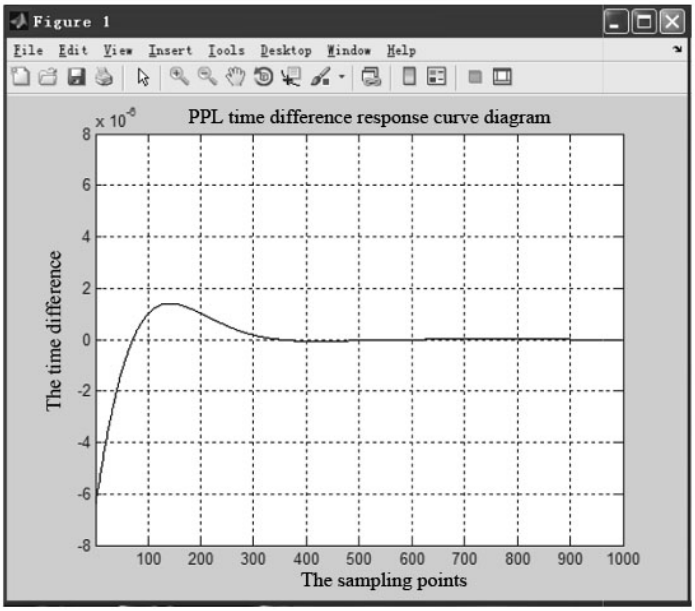


**Fig. (7).** The time difference between output and input signals.

$c2 = 0.00024722$ . The Matlab is used to do simulation, and the result is shown in Fig. (**6**).

The loop is locked at the position around the 350th sample point, the tracking time is about 40 ms. Based on FPGA, Costas loop is used to do time demodulation to IRIG-B(AC) code, after running for about 40ms starting from reset, the phase difference between input and output begins to approach zero. Because the ongoing process is an issue about time accuracy, it is necessary to convert phase difference to time difference. Because,

$$w = 2\pi f = \Delta\phi / \Delta t \tag{8}$$

$$\Delta t = \Delta\phi / 2\pi f$$

Hereinto, $w$ is the angular rate (rad/s), $\Delta\varphi$ is phase difference (rad), $\Delta t$ is time difference (s).

Thus the phase difference can be converted into time difference, the time difference between the input and output is obtained. Matlab is used to do the simulation and the results are shown in Fig. (**7**). From Fig. (**7**), it is shown that after tracking for about 40 ms, the time difference between output and input approaches zero. Costas loop can improve the decoding accuracy of IRIG-B(AC) to reach μs level to satisfy the requirement of the electric power system.

## CONCLUSION

Presently, plenty of time synchronization systems use GPS as the synchronous clock source. GPS is the most mature positioning system, but because GPS is controlled by the US Department of Defense, it is not possible to guarantee the interests of Chinese users. High precision timing has an important role in the field of national defense, scientific research and power systems in China. Therefore, through the BeiDou system with independent intellectual property rights, higher precision can be obtained to meet the requirements for safer time information, to ensure scientific research. In the fields of aerospace, communications, power, the requirement for a time unified system is very high. The design and realization of time unified terminal with high precision and small volume becomes increasingly important. Based on the FPGA IRIG-B (AC) code timing system, in the IRIG-B code (AC) demodulation the full digital Costas loop is introduced, which can extract the zero-crossing information of B (AC) code, this avoids problems such as zero drift and pulse jitter, etc., which have existed in the past demodulation circuit while using zero-crossing detection, making the synchronization error between the recovery carrier and the input B (AC) code decrease to 1 μs accuracy. The advantages of using FPGA to do timing with IRIG-B encoding are high precision, complete data and performing without manual preset and the defect is a complex coding procedure.

## CONFLICT OF INTEREST

The authors confirm that this article content has no conflict of interest.

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