Evaluation of a Commercial PhotoDiode Array for Radiation Detectors Readout

F. Carrió^{*}, V. González, E. Sanchis and J.M. Blasco

Department of Electronic Engineering, University of Valencia, Spain

Abstract: The aim of the present work is the characterization of the new S8866-128-02 PhotoDiode (PD) array from Hamamatsu Photonics. This work includes the implementation of a readout system as well as electronic noise estimation in PDs under several conditions varying integration times and clock frequencies.

Keywords: Medical physics, photodiode array, hadrontherapy, readout electronics.

INTRODUCTION

This work is an approach to the characterization Hamamatsu commercial S8866-128-02 PD (128 pixels, pitch 800 μ m) [1] managed by its C9118-01 controller [2]. These new PD arrays are combined with signal processing integrate circuit for X-ray detection applications. To characterize this new PD array we have used a readout system based on a FPGA development board coupled to an ADC mezzanine board. After storage in memory, data can be pre-processed in a FPGA and readout the extracted data in a Visual Basic application through an Ethernet port.

Noise in transducers is one of the main causes of the limitation for the final space resolution on the overall detector. Because of this, it is important to know the amount of electronic noise versus the integration time in the PD. This is the reason why we focus the results on this point. The performance of these new commercial PDs in such application depends on how noisy they are. The estimation of its *SNR* is then mandatory.

SYSTEM OVERVIEW AND READ-OUT SCHEME

Fig. (1) shows a view of the commercial PDs under study and its controller.



Fig. (1). View of the PDs (left) and its controller (right), both from Hamamatsu.

The setup used to readout the PDs is based on a Spartan3A DSP development board from Xilinx [3] and an EXP ISM Analog I/O Module from Avnet [4].

In Fig. (2) we show the block diagram of the electronics setup needed for the readout of the detector. As it can be seen, data coming from PD Driver is digitized by ADC Module and sent to the FPGA development board. The digitized data is stored into the internal memory prior to send it to the Visual Basic application through an Ethernet port. A real-time pre-processing into the FPGA development board is also possible if needed.



Fig. (2). Block diagram of used system to characterize PDs.

Fig. (3) shows the flowchart of the electronics setup. FPGA development board manages the PD Driver configuration and determine when analog video signal is digitized by the ADC Module. Also it stores the data and controls the information flow to the Visual Basic application.



Fig. (3). Flowchart of used system to characterize PDs.

^{*}Address correspondence to this author at the Campus Burjassot – Paterna, Avenida de la Universitat s/n - 46100 Burjassot (Valencia), Spain; Tel: +34 96354039; Fax: +34 9635 44353; E-mail: fernando.carrio@uv.es

EXPERIMENTAL SETUP

In order to conduct the PD tests we have developed a metallic box as detector prototype containing scintillating fibers over PD pixels 32 and 89 to 98, fibers have a pitch of 800 μ m matching the pitch of PDs pixels. The scintillating fibers have square dimensions of 0.5 mm x 0.5 mm and are from Kuraray Co. [5]. A 3 MBq activity Sr 90 radioactive source has been used as a charge injector for the detector prototype.

Fig. (4) shows the commercial electronic used for the tests.



Fig. (4). Pictures of the FPGA Spartan 3A DSP development board used for the tests (left) and the mezzanine board EXP ISM Analog I/O Module containing the Texas Instruments ADC for PD digitization (right).

Fig. (5) shows a picture containing the timing signals for the readout of one pixel. *ADC_CLK* is generated as a master clock from the Spartan board. A *reset* signal (not seen in the figure) from the board serves to initiates the integration time (charging integration) of the PDs. *Trigger* signal coming from the controller indicates *video* valid to the ADC. During this interval, the ADC digitizes the video signal coming out from PDs using *sampling* signals. Several samples/event can be used (in this particular case we show four samples/event), however for data taking we have used only one sample/event in order to avoid multiple switching on the PD controller and so trying to minimize the noise.

At bottom we show data after digitization.



Fig. (5). Main timing signal for a pixel readout.

In Fig. (6) we show a view of the box built as a detector. Inside, we have placed the fibers and the PD array.



Fig. (6). View of the box used as detector prototype.

Fig. (7) is a picture of the complete setup built for the tests. On the left, it can be seen the FPGA and mezzanine ADC boards. In the middle it is the PD Driver. On the right, the box containing the detector connected through a 10 cm flat cable to the PD Driver which will be outside the box. On the top the radioactive source used for charge injection is shown.



Fig. (7). Details of the experimental setup used for the tests.

RESULTS

A pedestal run allows us to estimate the electronic noise in the target pixels. In Fig. (8) we show pedestal results for a wide range of PD light integration time from several microseconds up to two seconds varying PD Driver clock frequency. As it is shown, noise remains quite reduced and almost constant up to integration times of 1s in agreement with Hamamatsu's results. For higher integration times the system becomes noisy.



Fig. (8). Noise standard deviation for different integration times.

The results of pedestal runs shown in Fig. (8) correspond to different integration times and PD Driver clock frequencies. Results obtained gave a pedestals of around 150 mV (about 1000 counts out of 65535) and an electronic noise of σ =5 mV for a video signal range of 3.3V. It should be noted that Hamamatsu's electronic noise results are around 1.1mV for low gain and 2mV for high gain using a PD clock frequency of 50 kHz and an integration time of 1ms in dark state.



Fig. (9). Noise standard deviation for different integration times.

After the electronic noise estimation, tests have been done in pixel 32 and pixels 89 to 98 putting a radioactive source on the target pixel. In the Fig. (9) we can see the results of the first setup placing the radioactive source on pixel 32.

As it said before, there is only scintillating fiber on pixel 32 so that is the reason why there is not signal on pixels 31 and 33. A change in the pedestal value gives negative values at pixels 31 and 33 for integration times higher than 1s.

In the Fig. (10) we can see the results of the second setup placing the radioactive source on pixel 95.

As it has been explained, there are scintillating fibers on pixel 89 to 98. As it is shown in the figure, there is signal on adjacent pixels to pixel 95. These non-expected signals are present because some part of the beam energy is transferred to the neighbor fibers due to the proximity between fibers and the aperture of the radioactive source and represents a crosstalk. We can note a good linearity over a wide range of integration times.

Fig. (11) shows a Visual Basic application to read these data. This application receives, through UDP port, the extracted data from FPGA development board, represents it on a bar graph and save it in a *csv* archive for a later analysis.



Fig. (10). Noise standard deviation for different integration times.



Fig. (11). Visual Basic application.

CONCLUSIONS AND FUTURE WORK

This kind of PDs is an alternative for readout instead of CCDs. The measured SNR is between 14 and 20 dB which is high enough to be used for the foreseen application. This measure is around at least 3dB more than CCD SNR, so these sensors provide an improvement of SNR. In terms of ENC it represents about 6.5 Ke⁻ to 13 Ke⁻ depending on the gain mode (high/low gain) we operate in the PD Driver.

Some work on signal integrity is needed in order to operate the PD Driver at the maximum 2.5 MHz allowed frequency and then minimize the dead time due to the electronics.

On the other hand, we are developing an embedded webserver with MicroBlaze [6] to access extracted data via http protocol. It will replace the Visual Basic application and will contain bar graphs and data statistical calculations.

Several applications of this work in the domain of medical physics are foreseen. In particular, *in vivo* dosimetry for irradiation control in radiotherapy, as well as precision beam profile for future hadrontherapy accelerators are some examples.

Received: May 15, 2011

Revised: September 29, 2011

Accepted: November 20, 2011

© Carrió et al.; Licensee Bentham Open.

This is an open access article licensed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/3.0/), which permits unrestricted, non-commercial use, distribution and reproduction in any medium, provided the work is properly cited.

ACKNOWLEDGEMENTS

Authors want to thank the aid given by M. Haguenauer and P. Poilleux from IN2P3 (Palaiseau, France) during the tests of the PDs and also to C. Marín and J. Torres from University of Valencia for their technical support.

CONFLICT OF INTEREST

None declared.

REFERENCES

- Hamamatsu Photonics, "Photodiode arrays with amplifier", Datasheet, Apr. 2010.
- [2] Hamamatsu Photonics, "Driver circuit for photodiode array with amplifier C9118 series", *Datasheet*, Feb. 2005.
- [3] Xilinx, "Spartan-3A DSP Starter Platform User Guide", User Guide UG454, Jan. 2009.
- [4] Avnet, "EXP ISM Analog I/O Module Manual", Manual, Oct. 2006.
- [5] http://www.kuraray.co.jp/en/
- [6] Xilinx, "Embedded system example: web server design using microblaze soft processor", Application Note XAPP433, Oct. 2006.