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Improved Reliability and Functionality of Clock Networks in ULSI Devices Due to Lossy Transmission Line Modeling Method

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Abstract: In this paper, the ways to improve the functionality and reliability of Digital Signal Processors, used to support optical networks, have been studied. Specifically, supported on our finding from previous experimental studies that on-die global interconnects should be described by a distributed *RLC* model, we propose to model shielded lines, carrying the most critical signals, by a Lossy Transmission Line (LTRA) model. The proposed method obviates the need for tedious simulations, which also due to many inevitably required oversimplifications have a low correlation with a real circuit behavior. The SPICE simulated signal waveforms obtained at the far-end of shielded lines correlate well with experimentally measured waveforms within a typical 45 nm CMOS technology ULSI chip. Based on both, simulations and experimental measurements, we have construed criteria whereby we modified the CMOS driver strength selection guideline to conform to the distributed nature of on-die interconnection lines. The performed simulations on a multi-level clock H-tree structure from a high-performance core block indicate that the new approach considerably improves MOSFETs reliability and power dissipation.

Keywords: Distributed properties of on-die interconnects, modeling of on-die shielded lines, on-die clock distribution network, CMOS driver strength optimization, reliability of ULSI devices.

INTRODUCTION

The phenomenal success in electro-optics and microelectronics within the last few decades has revolutionized the world of electronics and dramatically changed humans' daily lives. Different industrial segments, such as healthcare, telecommunication, aviation, Internet, automotive, and information cannot substantially advance without these multidisciplinary technologies. At the present, both electro-optics and microelectronics are tightly spliced together, and therefore they are naturally interdependent. The semiconductor microchips (also known as integrated circuits (ICs)) that lie at the heart of microelectronics are utilized in almost all electronic equipment in use today starting from toys and electronic games, ending with sophisticated computers, mobile phones and satellites. Equally important, the microchips are widely used in many critical optical devices. This is best exemplified by modern wireless access (WA) systems, which consist of radio frequency (RF) part, baseband part, control part, and transport part. The RF part receives data from the end users and converts it into the digital form, the baseband part processes it and outputs to terrestrial network trough the transport part. The entire process is controlled by the control part. The transport occurs via an optical network due to its high quality and high capacity. The baseband function is supported by powerful Digital Signal Processors (DSP) blocks, which are complex ULSI microchips implementing high frequency synchronous design. In these systems, the accurate functionality of the optical network, an essential and critical part, strongly depends upon reliability of the DSP.

In state-of-the-art microchips, employed in the above described systems, there is a need that signals be transferred over relatively long distances, up to a few millimeters. The ever-increasing operation speed of a microchip is one of the characteristics of microelectronics. Therefore, the bandwidth of on-die digital signals has been steadily expanding (i.e., the signal rise-times has been getting faster). The relation between the signal flight time (i.e., the time that takes to signal to propagate from one end of the line to another) and signal-rise time defines whether the line is distributed or lumped. A number of theoretical works concluded that the lines are distributed if signal double flight time is larger than signal rise-time. The same figure of merit determines the range of length of interconnection line in which its inductance should be taken into account [1]. At the same time, these works suggest the line is called lumped if signal flight time is ten times smaller than signal rise-time. Please note that in modern ULSI design, even lines of relatively long lengths have been traditionally modeled by a lumped *RC* model.

In our previous experimental studies based on a 45 nm CMOS technology typical ULSI test chip it has been shown that interconnection lines with circa 0.5 mm length and longer cannot be considered any more as lumped lines, since the effects pertained to distributed lines were plainly observed [2, 3]. At the same time, the present classical ULSI design approach says that in order to shorten the signal-rise-time (i.e., increase the operating speed) and to mitigate signals cross-coupling noise influence, the driver strength is required to be increased and the line length is required to be limited. The driver strength increase is usually achieved by either increasing the MOSFET channel width or decreasing the MOSFET channel length (if original length is bigger than the minimal channel length allowed by design rules of a

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specific technology node). Our experimental studies reveal that selecting the driver strength by this approach, accurate for lumped lines described by a *RC* model, may result in selection of a stronger or weaker than necessary driver (i.e., the overdrive or underdrive, respectively). It has been shown that signals passed through the typical on-die interconnection lines driven by a stronger (weaker) than necessary driver contain voltage overshoots (slowed-up slop), which are characteristic for distributed lines [3].

Our previous studies on device reliability, using Berkley Reliability Tools (BERT) model, have revealed that these corrupted signals, supplied to the input of the far-end CMOS logic cells, are a serious reliability concern since as a result the Time-Dependent Dielectric Breakdown (TDDB) and Negative Bias Temperature Instability (NBTI) wearout mechanisms are considerably aggravated [4]. Experimental evidences show that the lifetime of MOSFET devices with ultrathin oxides defined by the TDDB, follows a power-low relation with the gate-to-source voltage [5]. Hence, even small rapidly decaying overshoots in the gate voltage give rise to large changes in the device lifetime. The NBTI stresses primarily PMOSFETs, and the lifetime defined by this wearout mechanism has an exponential relation with the oxide electric field [6]. Consequently, voltage undershoots (during the signal transition from "high" to "low" logic levels) caused by an overdriven driver accelerates the device degradation as well. The unnecessary stronger driver not only affects the far-end CMOS logic cell reliability, but, as our study shows, the reliability of the driver itself is also seriously exacerbated [7]. The driver strength influences the shape of capacitive load current and impact ionization current. These currents, in their turn, define the device lifetime defined by the Hot Carriers Injection (HCI) wearout mechanism. Moreover, the signals at the driver output also may contain voltage overshoots. Even though latter have much lower amplitude with regard to those at the far-end they aggravate the driver reliability due to NBTI [8].

It is evident that the selection of the driver strength is very critical. To achieve this, the precise modeling is essential. The on-die interconnection lines, constituting signal distribution networks in modern ULSI devices, form very cumbersome and branching multilevel structures. The number of interconnects within ULSI chips is rapidly growing. Hence, their modeling even using a lumped *RC* model, let alone a distributed *RLC* model, that has to be used as experimental evidences suggest, is a very tedious and nontrivial task. The situation is just exacerbated in view of difficulties to accurately extract the inductance value. This topic is under intensive research and has been discussed in many theoretical works. Today, a comprehensive model of the entire interconnects network would consist of millions of sub-circuits. Such models cannot be processed by any currently available computational resources. Hence, today's models either take into account the very small area (lateral and vertical dimensions) of the modeled networks or comprise deficient amount of parasitic components (resistance, inductance, and capacitance). Moreover, there is no tangible figure of-merit regarding the minimum number of elements that could guarantee correct results. This casts doubts about the accuracy of the results and hampers the ability to perform the optimal design of signal distribution networks (e.g. determine the proper driver strength). The significant process variations just more diminish the correlation between simulated results and the subsequent real circuit behavior. At the same time, the utilization of an accurate model is becoming particularly important in view of continuous reduction in on-die supply voltage and threshold voltage of CMOS transistors that makes them very vulnerable.

These trends necessitate the developments of novel modeling approaches. This work is aimed at addressing this hitherto untouched issue, thus naturally guaranteeing the accurate functionality of many critical optical systems where the microchips are employed. In this paper, we propose to model the so called on-die shielded lines (utilized for clocks, controls, and other very critical signals where coupling noises should be eliminated or sufficiently mitigated) using the Lossy Transmission Line (LTRA) model. It is well known that any periodic *RLC* element may be regarded as a transmission line. The majority of on-die interconnects, however, are not implemented as transmission lines, since they do not have a continuous reference line, and therefore cannot be modeled as transmission lines. The shielded lines, on the other hand, are originally configured as transmission lines of a stripline structure. Therefore, these distributed lines can be modeled as transmission lines. The proposed in this paper modeling method obviates the need for tedious simulations, which due to many oversimplifications have a low correlation with a real circuit behavior. The complex problem of interconnects modeling, described above, does no longer arise and this is achieved without any element truncation, since transmission line has only one parameter, characteristic impedance. According to our simulations performed on a multi-level clock H-tree structure from a high-performance core block, the method helped significantly improve the reliability of ULSI MOSFETs and power consumption of a ULSI device in general owing to correctly selected driver strength using a modified by us guidelines, which conform to the distributed nature of on-die interconnection lines. All results are presented and discussed in the rest of the paper.

Background

Transmission lines, consisting of rectangular shape conductors, may be constructed in different ways, such as coplanar, stacked pair, diagonal pair, microstrip, and strip configurations. In the stripline configuration, a conducting strip is centered between two conducting ground planes, and the entire region between the ground planes is filled with a dielectric. The width of the strip, its thickness, and the relative permittivity of the dielectric define the characteristic impedance of the transmission line (we will refer to this important parameter later). The stripline, similarly to a coaxial cable, is non-dispersive, and a good isolation between adjacent traces is achieved. A typical stripline structure for readers' convenience is shown in Fig. (**1**).

The ULSI design uses the standard practice of so-called shielded lines, mainly employed to transfer the clock or control signals, and other most critical signals, where coupling noises should be eliminated or sufficiently mitigated. The shield is usually combined by AC ground (not switching) lines running in the same metal layer in parallel to the shielded line. The effectiveness of the shield mainly depends on a distance between the shield and the line, and it usually

decreases when the distance to the shield is larger than tree times the minimal distance between two adjacent metal lines in the same metal layer. The distance is set by a design rules and it varies from process to process. From the above description it follows that the shielded clock signal line is actually a classical stripline rotated by 90 degrees, and therefore all transmission line design rules, parameters' calculations, and modeling attitudes may be successfully applied. Given the appreciable level of (ohmic) resistive losses the on-die transmission lines cannot be considered as lossless lines [9]. Therefore, the Lossy Transmission Line (LTRA) model should be used.

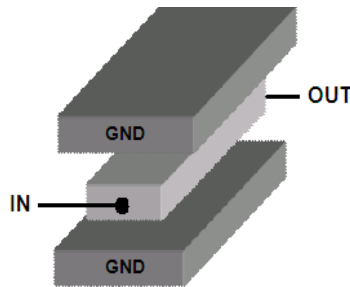

Fig. (1). A typical stripline structure. The signal line runs between 2 reference plates.

Fig. (**2**) presents the equivalent circuit of a typical on-die shielded clock line. The CKIN is the external (to our specific circuit) clock signal input, whereas CKOUT is the external (to our specific circuit) clock signal output. The driving and receiving CMOS inverters (so called clock buffering devices) are denoted in the scheme by X1 and X2, respectively. The CK1 and CK2 are the probing points of the shielded clock signals, and are located at the driver output (near-end) and receiver input (far-end), respectively. The clock signal line is shown as the transmission line T1. The capacitor C_{load} represents the capacitive load, introduced by the receiver (X2) gate capacitance. The inset in Fig. (**2**) conceptually shows the 3-dimentional structure of the shielded clock line fragment, where shields at both sides of the signal line are connected to ground.

LTRA MODEL *VS*. LUMPED RC MODEL

As it has already been mentioned in the introduction section, the use of an accurate interconnection lines model is very crucial for the proper selection of the CMOS driver strength, which in its turn has a strong impact upon correct logic functionality as well as signal integrity, device reliability and power consumption. The present ULSI design approach says that in order to shorten the signal-rise-time (i.e., increase the operation speed and reduce susceptibility to power supply and ground noise), the driver strength is just required to be increased, and a driven interconnection line can be modeled using a lumped *RC* model. For readers' convenience, to accentuate the extent of discrepancy between the lumped *RC* model and LTRA model (the model that should be used according to findings and conclusions of our previous experimental studies) we compare signal waveforms obtained, using SPICE simulator, at the far-end of a 0.5 mm length shielded line driven by a CMOS driver with a variable strength for both models (see Fig. **3** and Fig. **4**). Please note, that in both models we used the same driver strengths. Fig. (**3**) (*RC* model) shows that with the increase of the driver strength by a factor of 2 and 4, while keeping the same length of a driven line, the signal rise-time becomes by 28% and 38% faster, respectively. Please note that the waveforms are different from each other by rise-time only. The voltage scale in this figure was normalized with regard to supply voltage. The waveforms in Fig. (**4**) (LTRA model) are substantially different from those in Fig. (**3**), and not only by considerably different rise-times. Moreover, it is easily discerned that the change in the driver strength has a very strong impact upon the shape of a waveform, which is a very characteristic for distributed lines. For instance, when driver strength is insufficient (known as underdrive) a signal becomes "undulating" due to slope changes resulting from bouncing of waves with different amplitudes back and forth along the line. Each slope change is caused from the next reflection. Overdriving the line causes voltage overshoots (~14 % in the given case) and ringing back. The overshoot amplitude strongly depends on the extent of the overdrive. These distinctive attributes in signal waveforms stem from the fact that in a distributed line the initial voltage wave is based on a voltage division between driver output impedance and characteristic impedance of a driven line, and is below (above) a half a supply voltage in underdriven (overdriven) case. The waveforms in Fig. (**4**) correlate well with experimentally obtained signal waveforms from a ULSI test chip based on a 45 nm CMOS technology (see Fig. **5**). Very small differences in the waveforms are easily explained by ideal conditions and certain simplifications intrinsically assumed in SPICE simulator, as well as measurement accuracy limita-

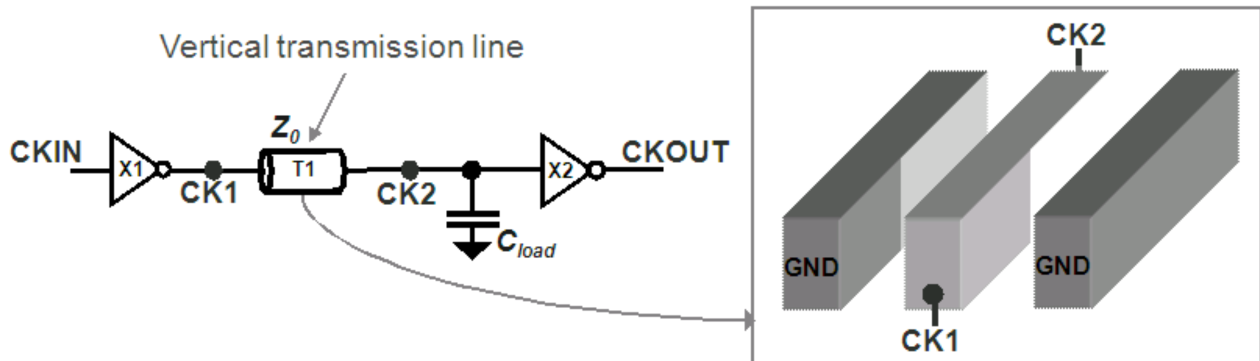

Fig. (2). Schematic diagram and the physical structure of the shielded interconnect line in a ULSI chip. The shielded line is in essence a stripline, rotated by 90 degrees.

tion. A detailed description on our experimental studies as well as elaborated discussions on this topic in general and impact of overdrive and underdrive upon device reliability in particular can be found elsewhere [3, 4].

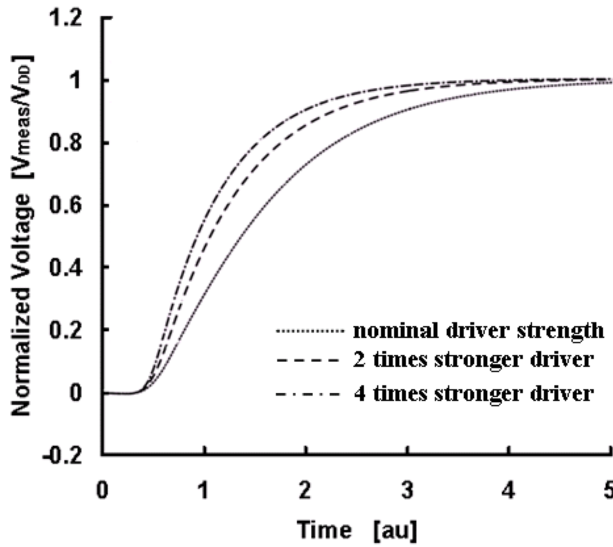

Fig. (3). SPICE simulated signal waveforms (45 nm CMOS technology), using a lumped RC model, at the far-end of a typical on-die shielded line. The different curves correspond to different strengths of the CMOS driver. The voltage scale was normalized with regard to supply voltage.

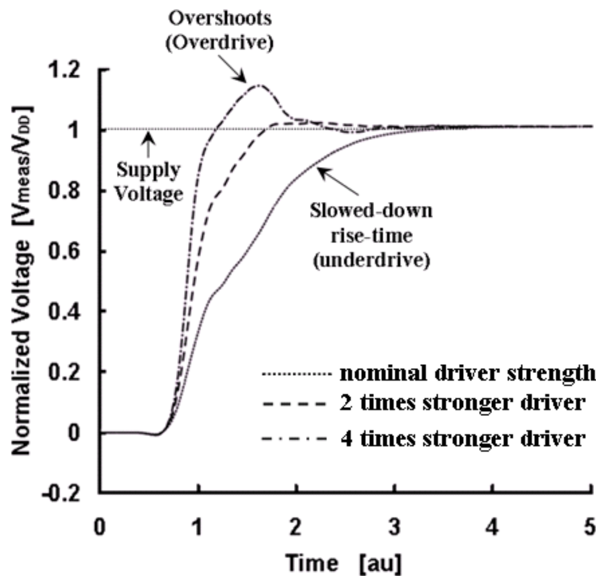

Fig. (4). SPICE simulated signal waveforms (45 nm CMOS technology), using a distributed RLC model, at the far-end of a typical on-die shielded line. The different curves correspond to different strengths of the CMOS driver. The voltage scale was normalized with regard to supply voltage.

CMOS DRIVER STRENGTH OPTIMIZATION

From the presented above it is clear that the CMOS driver strength selection based on the currently existing

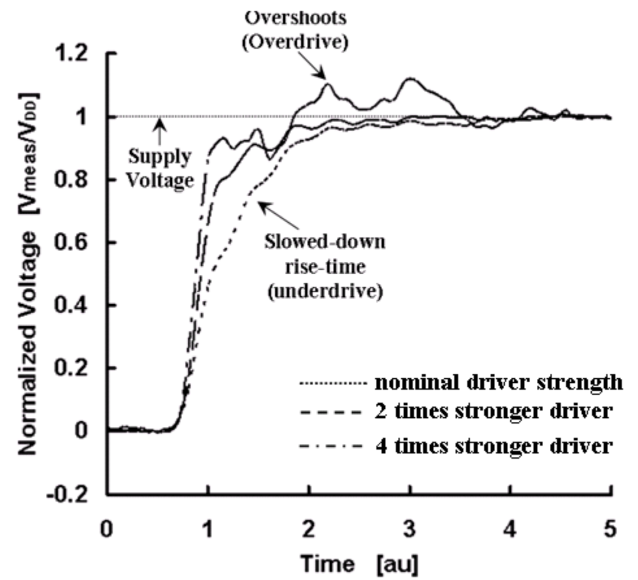

Fig. (5). Experimentally obtained signal waveforms (45 nm CMOS technology), using a microprobing technique, at the far-end of a typical on-die interconnection line. The different curves correspond to different driver strengths. The voltage scale was normalized with regard to supply voltage.

approach is no longer practicable, and should be revised. In classical transmission lines design, such a procedure is known as impedance matching. That is, the selection of driver strength is done in such a way that driver output impedance matches the characteristic impedance of a driven transmission line. The accurate impedance matching is possible only if all parameters are well characterized and stable. In ULSI applications, however, where some parameters are not known and are not repeatable, this process is not trivial. The situation is just getting more complicated in view of the on-die lines' ohmic (resistive) losses, which have been growing due to continuous dimensions downsizing. These losses, according to the transmission line theory, makes the characteristic impedance of transmission line, reflection coefficient, and signal propagation constant frequency dependent, whereas the spectrum of transmitted clock-like and other digital signals consists of many harmonics. Furthermore, the CMOS driver has a non-linear behavior during its switching. Since the MOSFET's channel build-up has a finite time, the signal generation and subsequent propagation down the line begins long before the channel is completely built. The switching driver output impedance is changing during the channel build-up process. Moreover, given that signal rise-time is larger than double signal flight time, the reflected signal from the far-end arrives before the completion of the build-up process, and superimposing with the driver output voltage, additionally and unpredictably modifies the driver output impedance. Fig. (**6**) conceptually presents this non-linear effect. Actually, the driver may be presented as ideal driver with an additional serial resistor, which changes during the signal propagation. This effect requires special attention while selecting the driver strength. From the above it follows that an attempt to match the impedances based on the statically calculated MOSFET's channel resistance may result in an appreciable discrepancy with regard to the real situation.

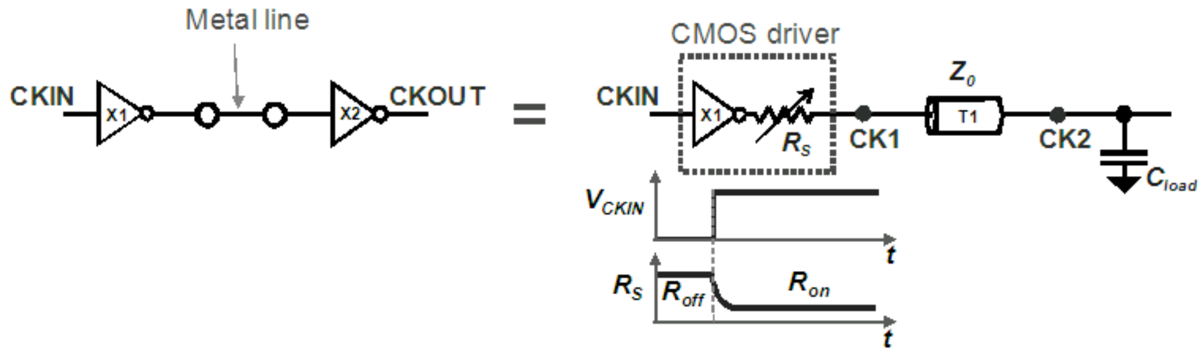

Fig. (6). Schematic representation of the driver-line-receiver structure. In reality the driver has a varying during its switching output impedance, and the line is a lossy transmission line terminated in open-circuit (gate of the CMOS receiver).

Despite the difficulties with the estimation of the driver output impedance, the use of transmission line model enables to easily determine whether the driver strength is sufficient. The fundamental theory of transmission lines explicitly states that overshoots begin to appear when the source impedance becomes smaller than that of the driven line. We can use this condition as a marker to track the driver's transition into overdrive. It should be noted that in our previous studies it was found that the insufficient driver strength (underdrive) also hurts the device reliability due to HCI wearout mechanism, increases power consumption, and leads to logic instabilities. Thus, the underdrive should be avoided, and using overshoots as a figure of merit can be avoided as well.

While seeking for the optimal driver strength, designers actually strive to obtain the fastest voltage transition (i.e., the shortest signal rise-time) in slowest Process/Voltage/ Temperature (PVT) case. This decreases energy loss due to the crowbar current in the loading (i.e. next) CMOS stage. This also allows to decrease as much as possible the signal distortion in the clock signal electrical path due to process variation and supply or substrate noise, both inside the CMOS driver and between CMOS driver and the load. The fastest transition approach is a well established approach that is allowed and well supported by standard Electronic Design Automation (EDA) software tools. Based on this approach, well suited for lumped *RC* lines, the driver strength can be adjusted in the "era" of distributed lines, as well. However, differently from a lumped *RC* model there must be an upper limit for the driver strength. Standard approach limits the driver strength mainly based on growing (with the driver increase) its input capacitance, which can load the predeceasing signal stage, and partly by areal constraint. However we state that this limit should be the strength at which the voltage overshoots begin to appear. That is, the onset of overshoots corresponds to the proper driver strength.

IMPLEMENTATION OF A NEW GUIDELINE

The ULSI design often uses the special clock distribution network arrangement, called symmetric clock tree (A.K.A. H-tree) with shielded lines (see Fig. **7**). This technique is known of providing the low skew and low noise clock in high performance functional units [10]. It should be noted that the clock signal is the most critical signal in an entire microchip. The integrity of the clock has a very strong impact upon the logic functionality of all functional units. The clock tree may use 2 different approaches or their mixture. The first approach defines H-tree creation with no buffering CMOS stages at the clock tree vertexes (i.e., without the insertion of active repeaters). This approach is applicable for small clock trees. The second approach requires some kind of buffering and is used for large clock trees. Buffering of a clock signal, propagating through the clock tree, allows better signal integrity, but of course has subtle shortcomings, such as larger clock signal propagation delay and power consumption.

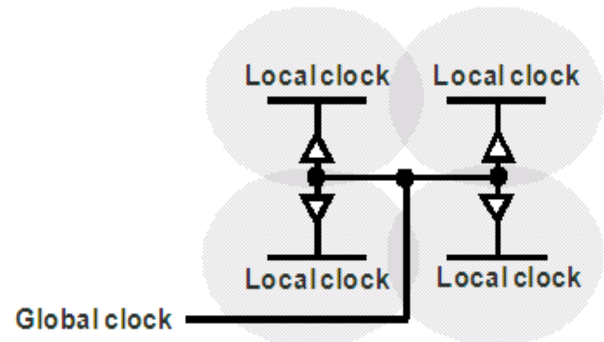

Fig. (7). The schematic diagram of the symmetric H-trree structure approach. 2 repeaters are placed at the clock tree vertex to create point-to-point connection and ensure line-driver impedance matching. The local clock net is connected to all sequential components, located in the "cloud" or at its proximity.

In this study, we applied the described above revised guideline to optimize the clock tree drivers in a 1GHz running core block within a 45 nm CMOS technology node chip. The block, taken as an example for mentioned above clock tree design has a 6-level H-tree clock structure. The selection of the clock tree topology is usually based on the number of sequential components, fed by the clock signal. Since the number of the sequential components is very large, and a subsequently introduced, by these components, capacitive load is also high, several buffering stages (active repeaters) are required to provide the desirable signal transfer from its source to its final destination. The estimation of the optimal number of active repeaters is a standard procedure and is 1033 well supported by a variety of EDA tools. Specifically, such tools select the number of repeaters, based on a maximum allowed signal slope. The

repeater may be either inverter or buffer (2 inverters connected in series). Inverters introduce less circuit delay, but strong inverter is characterized by large input capacitance, that has backward influence, which is usually attempted to be avoided. Buffers have slightly bigger circuit delay, but are characterized by minimal input capacitance, and therefore usually preferred. In our case we use repeaters of a buffer type. Fig. (**8**) presents the topology of this clock tree. The Buffers, discussed above, are placed at the vertex of each clock tree stage. The driver strength was selected based on two criteria. First, according to fastest transition criterion in slowest PVT (also known as SS (slow-slow), high voltage, and at low temperature). The second criterion was the minimized overshoots' amplitude.

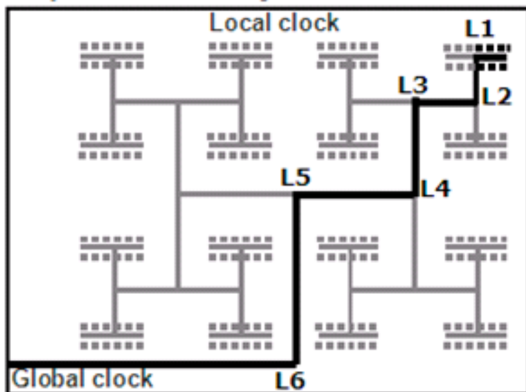

Fig. (8). A complete 6-level symmetric clock tree structure. Repeaters are placed at each vertex of the tree. Dots of the tree leaves schematically represent connection to sequential components located in corresponding proximity of the leaf.

Fig. (**9**) presents the group of signal waveforms, characterizing their behavior at vertexes of the clock tree described in Fig. (**8**). The first waveform corresponds to the signal, inputting the clock tree structure. The next 5 waveforms describe the clock signal propagation in the clock tree stage named L6. Following 4 waveforms represent the clock tree stages from L5 to L2. Than L1 stage (the last stage, which collects all sequential components in the local "cloud" of the circuit) is presented by 2 waveforms, referring to the clock signal point near the buffer and far away from the buffer. The following waveforms describe the clock signal behavior at different sequential components, which left out of the scope of this discussion.

From the waveforms presented in the figure it is evident that owing to the combination of the clock tree modeling using the LTRA model and selection of drivers strengths based on a proposed new guideline it is possible to avoid the excessive driver strength (overdrive) that incurs detrimental overshoots. The most signals have a desirable for correct logic functionality rise-time and are free of overshoots. A very few signals still contain overshoots, which is the outcome of process variations. This is, however, the intrinsic shortcoming of a SPICE simulator and of course requires further studies. It should be emphasized that the maximal overshoot monitored in fastest PVT corner (also known as FF (fast-fast), low voltage, and at high temperature) is only ~7% with regard to the nominal value. This is a half relative to overshoots observed in Fig. (**3**) (*RC* model).

IMPROVED RELIABILITY AND FUNCTIONALITY

A number of reliability models and simulation methodologies, such as the Berkeley reliability tools (BERT) [11], have been developed during the past decade for the modeling of device wearout. The actual device degradation is estimated by the BERT model as a function of the parameter called *Age*. The degradation is calculated from *Age* using empirical functions and lookup tables. The BERT simulation comprises a sequence of time intervals, in each of which, the degradation is estimated considering the obtained results from a previous one. The *Age* is calculated separately for each wearout mechanism (TDDB in our case) and is inversely proportional to the device lifetime defined by this mechanism. In this work, to qualitatively gauge the improvement of clock networks reliability owing to the proposed new guidelines, we compare the simulated *Age* parameters

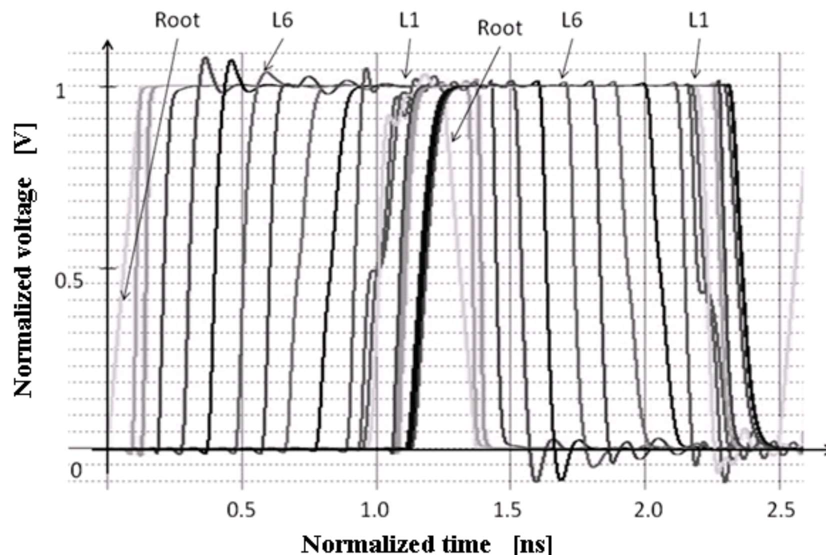

Fig. (9). Clock tree vertex signals' waveforms, obtained at all stages of the clock tree.

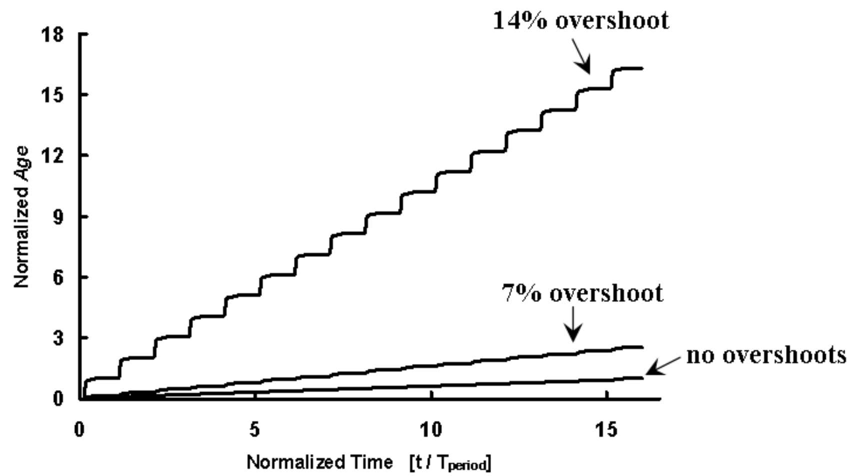

Fig. (10). Simulated Age parameter for the TDDB wearout mechanism as a function of time for overdriven cases with overshoot amplitudes of 7% and 14% and for a matched driver's strength (free of overshoots). The results were normalized so that at the end of the simulation period (corresponds to 16 periods of signal) the Age in a matched case is equal to 1 to accentuate the acceleration of the device degradation due to overdrive.

(from BERT model) of MOSFETs constituting a CMOS logic cell whose input is supplied with signals containing different levels of voltage overshoots.

The experimental evidence shows that the lifetime of MOSFETs as defined by the TDDB, follows a power-low relation with the gate-to-source voltage (lifetime$_{TDDB}$ $\propto V_{GS}^{-45}$) [5]. All operating MOSFETs inevitably experience a gradual shift of their electrical parameters (i.e., the aging). For properly selected driver, where signal is free from overshoots, the amount of *Age* of transistors, connected to the far-end of the line, grows gradually while they are in "on" state and remains constant while they are in "off" state. Therefore, for the clock-like signals, the *Age* curve over time gets the form of a staircase function with gradual increases. Given the lifetime definition, even small voltage overshoots, caused by the excessive driver strength, lead to a large increase in the *Age* parameter. Fig. (**10**) shows that for 7% and 14% overshoots, the *Age* is 2.53 and 16.3 times, respectively, faster with regard to the case where signal is not corrupted. The results were normalized in such a way that the aging in a matched case is equal to 1 at the end of the simulated period (16 periods of a clock signal).

Thus, the reliability of MOSFETs from clock networks is sufficiently improved owing to the proposed modeling approach. The latter is also conducive to decrease the excessive power consumption caused by the overdrive, as can be seen in Fig. (**11**). It is demonstrated that 14% of voltage overshoots result in 7.3% increase in power dissipation. It is worth mentioning that overshoots cause cross-talk noise to neighbor lines and power supply noise transmitted to other active elements utilizing the same power network. This, in turn, may lead to functional failure of latch devices. Our previous experimental studies on inter-symbol interference (ISI) revealed that overshoots aggravate this deleterious effect. The increase of the CMOS driver strength is achieved by increase in the width of MOSFETs constituting the driver. Hence, the introduction of the proposed new guidelines allows to reduce the driver size, thus saving scarce on-die routing resources. In some cases, in this study, the selected buffers size was shrunk by a factor of 2 and more.

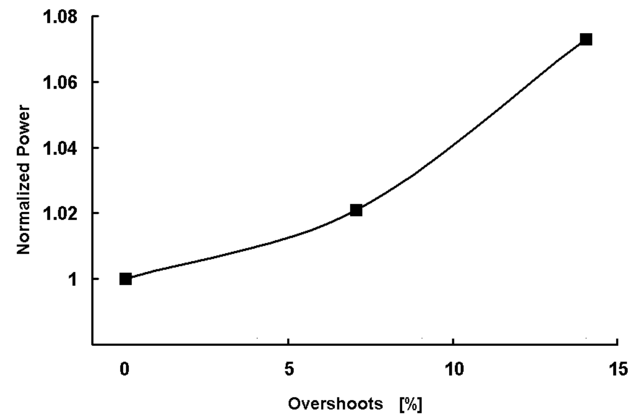

Fig. (11). The power loss in an overdriven case as a function of the overshoot amplitude, evaluated for a 45 nm CMOS technology process.

SUMMARY AND CONCLUSIONS

In this work, we proposed to model on-die shielded interconnection lines, aimed at carrying out clocks, controls, and other most critical signals, using the Lossy Transmission Lines (LTRA) model. Our previous experimental studies revealed that on-die interconnects of 0.5 mm length and longer behave as distributed lines, and therefore the traditionally used lumped *RC* model is no longer practicable. On the other hand, given the complicated structure of on-die interconnects' networks, it is unfeasible to precisely model them using distributed *RLC* models by currently available computer resources. The use of LTRA model obviates the need to make tedious simulations in which inevitably required oversimplifications result in a low correlation with a subsequent behavior of a real circuit. It should be noted that at the present time there are no additional practicable alternatives to the proposed LTRA model. This is particularly true in the view of a constant expansion of the digital signals bandwidth and growth of interconnection line lengths in ULSI microchips.

It has been shown that serious errors in the estimation of the required strength of CMOS drivers that drive distributed interconnection lines may occur if the strength is selected based on the fastest voltage transition (i.e., the shortest signal rise-time) in slowest Process/Voltage/Temperature (PVT) case, the method that has been successfully used for lumped interconnects described by a *RC* model. According to experimental studies, the excessive (insufficient) driver strength results in signal distortions, which are manifested as voltage overshoots (slowed-down rise-time). These distortions, which lead to excessive power dissipation of MOSFETs (constituting far-end as well as near-end CMOS logic cells) and substantial aggravation of their reliability, are easily detected while modeling by LTRA model. Hence, one can use the onset of overshoots as a marker to transition from insufficient to excessive driver strength (i.e., matched strength). Thereby, we propose to select the driver strength using the fastest voltage transition in slowest PVT case approach, but differently from a lumped RC model there is an upper limit for the driver strength. This limit should be the strength at which the voltage overshoots begin to appear.

In this paper it has been exemplified on a clock network from a typical DSP block that the new modeling method together with the modified CMOS driver strength selection guideline helped considerably improve signal integrity of clock signals, and subsequently avert reliability problems as well as power consumption waste. Thus, we conclude that these new approaches can be successfully integrated into modern ULSI design rules. Thereby, owing this method the functionality of critical optical networks where the micro-chips are used may be considerably enhanced.

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